# Field Effect Transistor and FET Amplifiers

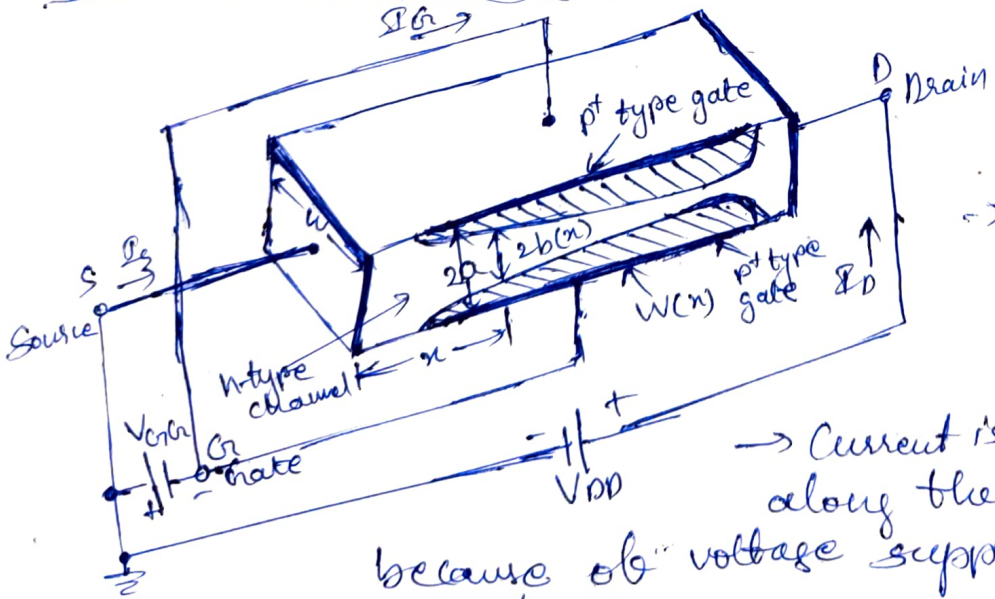
→ Field effect transistor is a semiconductor device which depends for its operation on the control of current by an electric field.

→ There are two types of field-effect transistors
- ↳ junction-field-effect-transistor (JFET or simply FET)
- ↳ insulated-gate-field-effect-transistor (IGFET), commonly called metal-oxide-semiconductor (MOS) transistor (MOSFET)

→ FET enjoys several advantages over the conventional transistors.
1) Its operation depends upon the flow of majority carriers only. It is therefore a unipolar (one type of carrier) device.
2) It is relatively immune to radiation
3) It exhibits a high i/p resistance, typically many mega-ohms
4) It is less noisy than tube or a bipolar transistor
5) It exhibits no offset voltage at zero drain current & hence makes an excellent signal chopper.
6) It has thermal stability

→ The main disadvantage of FET is its relatively small gain-bandwidth product in comparision with that of a conventional transistor.

## Junction Field-Effect Transistor




→ This is structure of an n-channel field-effect transistor

→ If p-type silicon is used, the device is referred to as p-channel FET.

→ Current is caused to flow along the length of the bar because of voltage supply connected b/w the ends of the bar.

→ This current consists of majority carriers which in this case are electrons.

Source :- The source S is the terminal through which the majority carriers enter the bar. → Conventional current entering this bar at S is designated by $I_S$

Drain :- The drain D is the terminal through which the majority carriers leave the bar.
→ Conventional current entering the bar at D is designated by $I_D$
→ The drain-to-source voltage is called $V_{DS}$ & is +ve if D is more +ve than S

Gate :- On both sides of n-type bar, heavily doped ($p^+$) regions of acceptor impurities have been formed by alloying, by diffusion or by any procedure for creating p-n junctions. These impurity regions are called the gate G.
→ B/w gate & source a voltage $V_{GS}$ is applied in reverse-the direction to bias the p-n junction.
→ Conventional current entering the bar at G is designated $I_G$.

Channel :- The region of n-type material b/w the two gate regions is the channel through which the majority carriers move from source to drain.

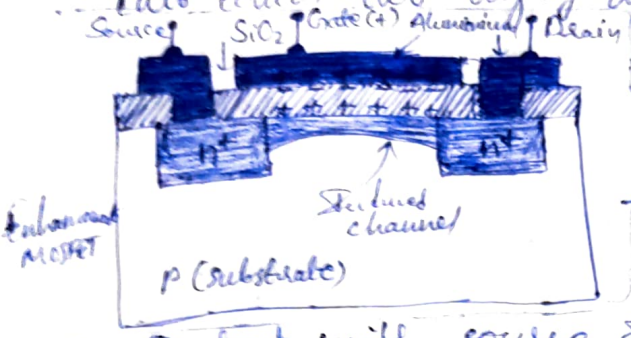
FET Operation
→ The two sides of the transition region of reverse-biased p-n junction there are space charge regions.
→ The electric lines of field intensity which now originate on the +ve ions & terminate on -ve ions are source of voltage drop across the junction.
→ As reverse bias across the junction increases, so also does the thickness of the region of immobile uncovered charges.
→ The conductivity of this region is theoretically zero because of unavailability of current carriers. Hence the effective width of channel will become progressively decreased with increasing reverse bias.
→ For a fixed drain-to-source voltage, the drain current will be a function of reverse-biasing voltage across the gate junction
→ The term field effect is used to describe this device because the mechanism of current control is the effect of extension, with increasing reverse bias, of field associated with region of uncovered charges

## Insulated-Gate FET (MOSFET)

or Metal-oxide-semiconductor FET

→ The insulated-gate FET have greater commercial importance than the junction FET

→ An n-channel MOSFET consists of a lightly doped p-type substrate into which two highly doped $n^+$ regions are diffused.




→ The $n^+$ sections will act as the source & drain, are seperated by about 1 milimeter.

→ A thin layer of insulating silicon dioxide ($SiO_2$) is grown over the surface of the structure, allowing contact with source & drain.

→ The gate-metal area is overlaid on the oxide, covering the entire channel region. Simultaneously metal contacts are made to drain & source

→ The contact to the metal over the channel area is the gate terminal.

→ The metal area of gate in conjunction with the insulating dielectric oxide layer & the semiconductor channel forms a parallel-plate capacitor.

→ Because the insulating layer of silicon dioxide, this device is called insulated-gate-field-effect transistor,

→ This layer results in an extremely high i/p resistance ($10^{10}$ to $10^{15}\,\Omega$) for the MOSFET.

**Enhancement MOSFET** :- If we ground the substrate for the above structure & apply a +ve voltage at the gate, an electric field will be directed ⊥ly through the oxide.

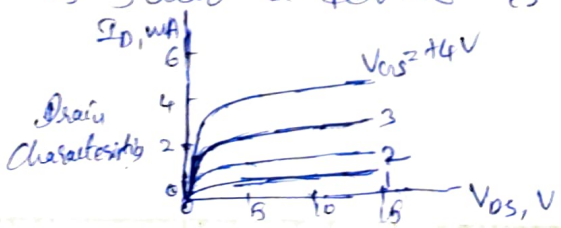
→ This field will end on "induced" -ve charges on semiconductor site.

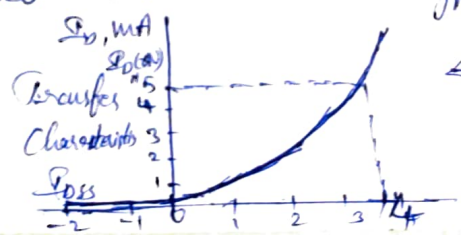
→ The -ve charge of electrons which are minority carriers in p-type substrate forms an "inversion layer"

→ As the +ve voltage on gate increases, the induced -ve charge in the semiconductor increases.

→ The region beneath the oxide now has n-type carriers, the conductivity increases & current flows from source to drain through the induced channel.

→ Thus the drain current is enhanced by the +ve gate voltage & such a device is called an enhancement-type MOS



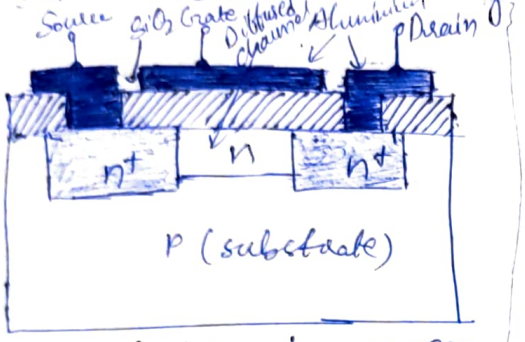

← of an n-channel enhancement-type MOSFET

## Depletion MOSFET

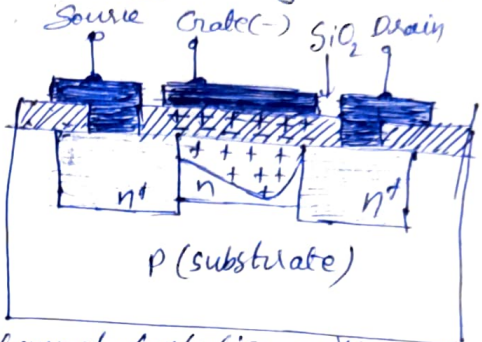
→ A second type of MOSFET can be made if an n-channel is diffused b/w the source & drain

→ With this device an appreciable drain current $I_{DSS}$ flows for zero gate-to-source voltage $V_{GS} = 0$

→ If the gate voltage is made -ve, +ve charges are induced in the channel through the $SiO_2$ of gate capacitor.




Depletion-type MOSFET



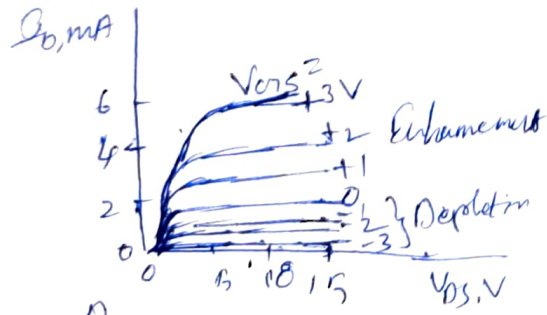

Channel depletion with application of a -ve gate voltage

→ Since the current in a FET is due to majority carriers, the induced +ve charges make the channel less conductive & drain current drops as $V_{GS}$ is made more -ve

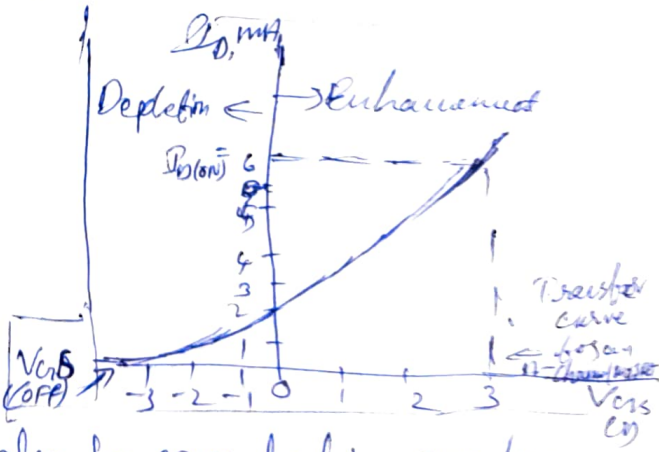
→ The redistribution of charge in the channel causes an effective depletion of majority carriers, which accounts for the designation depletion MOSFET

→ Because of the voltage drop due to drain current, the channel region nearest the drain is more depleted than the volume near source.

→ This phenomenon is analogous to that of pinch-off occurring in a JFET at the drain current near the source.




Drain characteristics

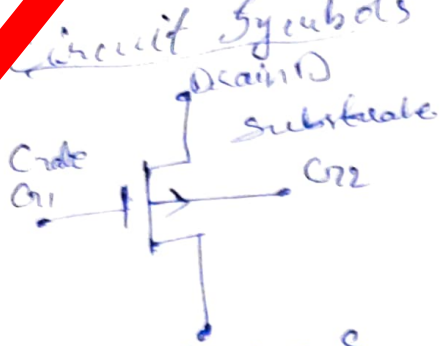


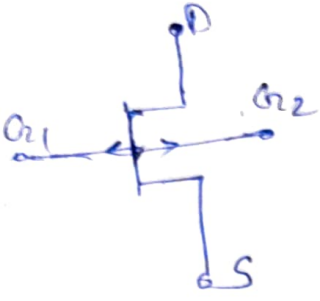

→ A MOSFET of depletion type may also be operated in an enhancement mode.

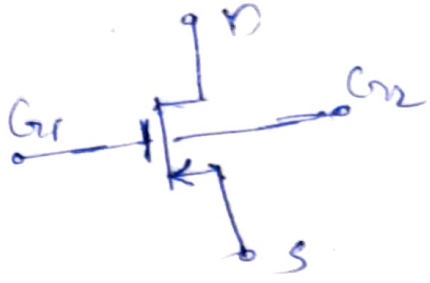
→ It is necessary to apply a +ve gate voltage so that -ve charges are induced into the n-type channel

→ In this manner the conductivity of the channel increases & the current rises above $I_{DSS}$

Circuit Symbols




p-channel MOSFET