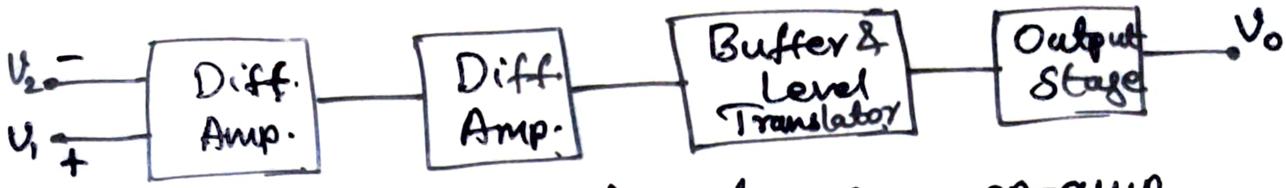
Operational Amplifier Internal Circuit



Block schematic of an op-amp

→ First two stages are cascaded differential amplifiers to provide high gain & high i/p resistance.

→ Third stage acts as buffer as well as a level shifter (translator).

↳ Buffer is an emitter follower whose i/p impedance is very high so that it prevents loading of high gain stage.

↳ Level shifter adjusts the d.c. voltages so that output is zero for zero i/ps.

→ Output stage is designed to provide a low o/p impedance.

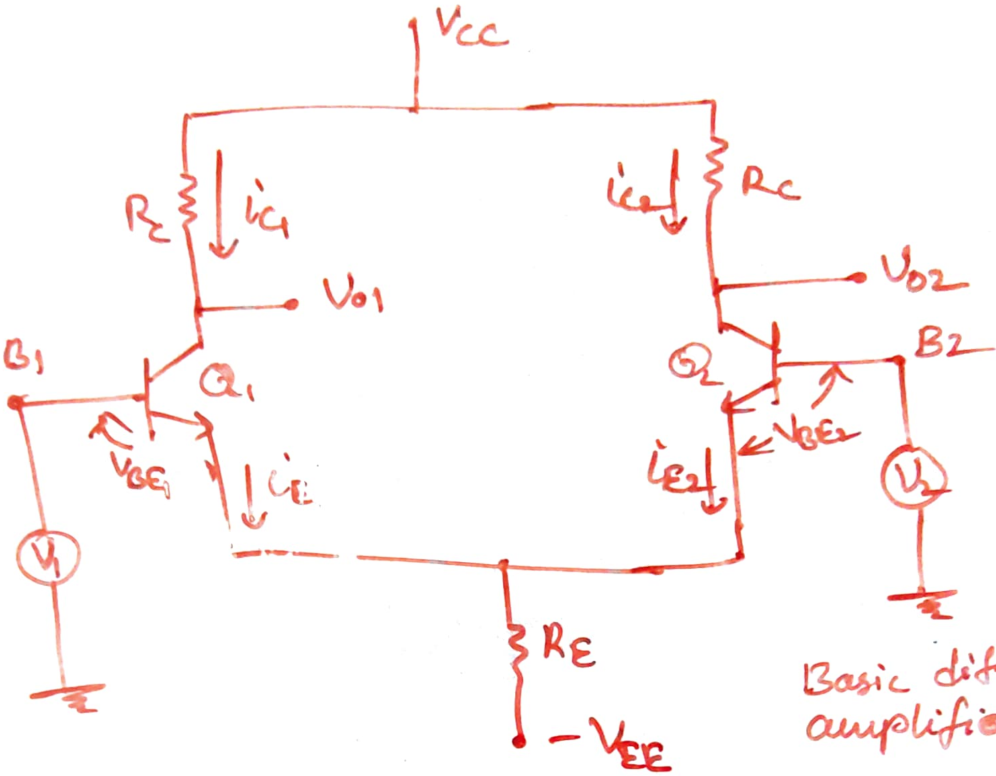
Differential Amplifier

→ To provide high gain to the difference mode signal and cancel the common-mode signal.

→ A cascaded direct coupled amplifier can provide high gain down to zero freq. as it has no coupling capacitor.

→ This amplifier suffers from drift of operating point due to temp. dependancy of I_{CO}, V_{BE} and h_{fe} of transistor.

→ This problem can be eliminated by using a balanced or differential amplifier which is emitter-coupled differential amplifier with low drift based on symmetrical construction.



Basic differential amplifier

→ This differential amplifier can be used in four different configurations depending upon the no. of i/p signals used and the way o/p is taken.

i) Differential-input, differential-output (or) Dual-input balanced output.

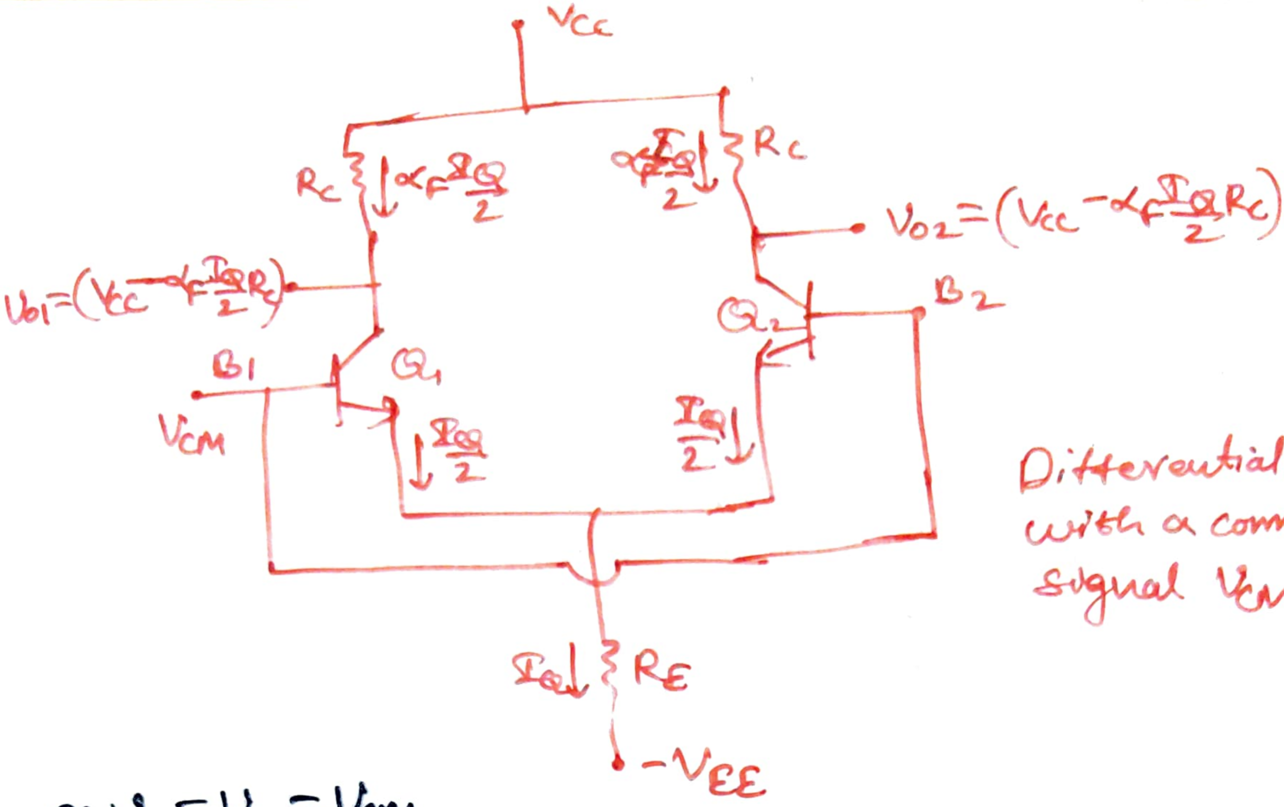
ii) Differential-input, single ended-output ~~(or)~~

iii) Single-input, differential-output

iv) Single-input, single ended-output

→ If signal is applied to ~~both~~ both i/ps, then it is differential i/p or dual i/p

→ If o/p voltage is measured between two collectors then it is a differential o/p or balanced o/p.



Differential pair with a common-mode signal V_{CM}

→ If $V_1 = V_2 = V_{CM}$

Q_1 & Q_2 are F.B and matched

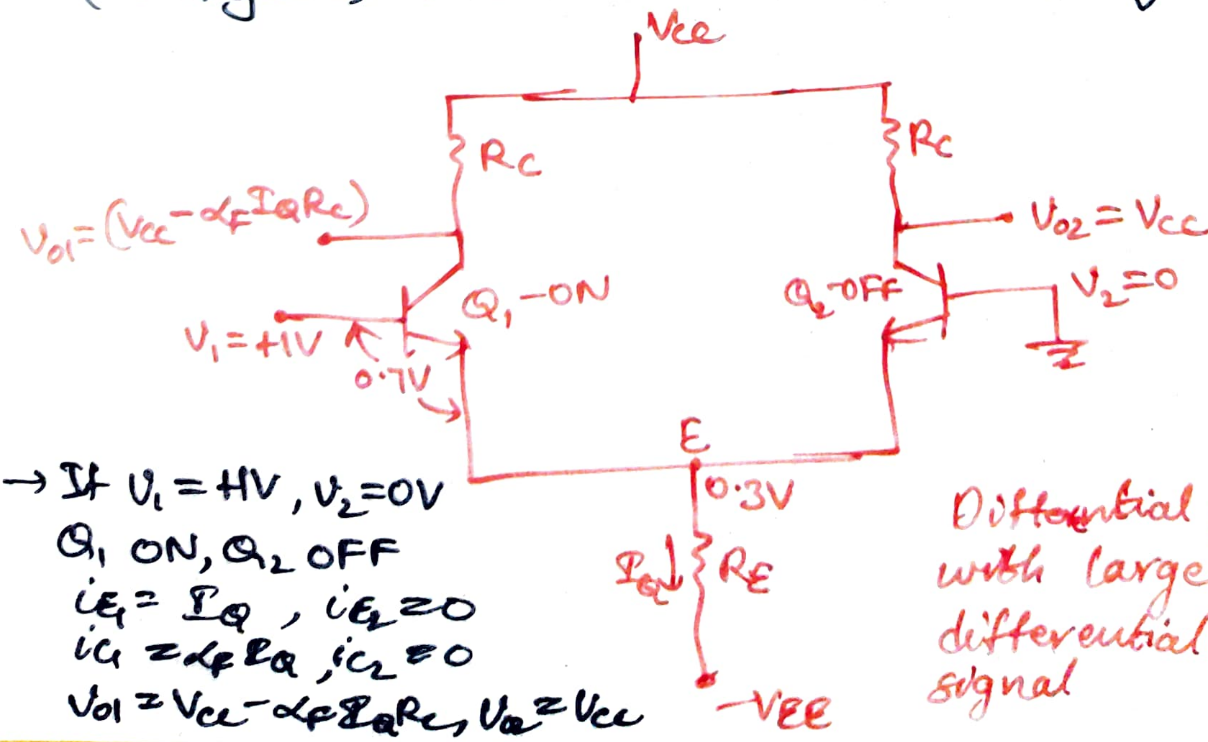
→ Due to symmetry of ckt, $i_{E1} = i_{E2} = \frac{I_Q}{2}$

$$i_{C1} = i_{C2} = \alpha_F \frac{I_Q}{2}$$

$$V_{o1} = V_{o2} = V_{CC} - \alpha_F \frac{I_Q}{2} R_C$$

$$V_{o1} - V_{o2} = 0$$

→ Thus, differential pair does not respond to (or rejects) the common-mode i/p signals.



Differential pair with large differential i/p signal

→ If $V_1 = 1V$, $V_2 = 0V$

Q_1 ON, Q_2 OFF

$i_{E1} = I_Q$, $i_{E2} = 0$

$i_{C1} = \alpha_F I_Q$, $i_{C2} = 0$

$V_{o1} = V_{CC} - \alpha_F I_Q R_C$, $V_{o2} = V_{CC}$

Output for Arbitrary Signals

→ If any arbitrary signals v_1 & v_2 are applied (other than $\frac{V_d}{2}$ or V_c), then these signals can be represented by sum & difference of V_{cm} ($= V_c$) & V_{DM} ($= \frac{V_d}{2}$) as

$$v_1 = V_{cm} + V_{DM}$$

$$V_2 = V_{cm} - V_{DM}$$

$$V_{DM} = \frac{V_1 - V_2}{2} \quad \& \quad V_{cm} = \frac{V_1 + V_2}{2}$$

$$V_{o1} = A_{DM} V_{DM} + A_{cm} V_{cm}$$

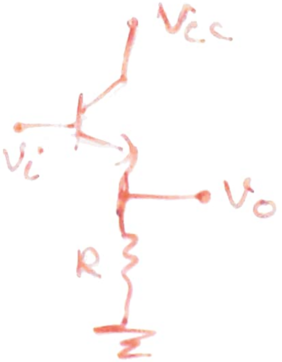
$$V_{o2} = -A_{DM} V_{DM} + A_{cm} V_{cm}$$

Level Translator

→ Because of direct coupling, dc level rises from stage to stage which tends to shift the operating point of next stage.

→ The o/p should have quiescent voltage level of 0V for zero i/p signal.

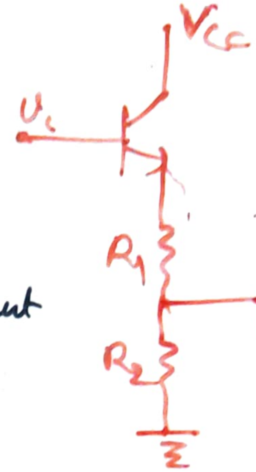
→ Basically an emitter follower is level shifter also acts as buffer to isolate high gain stages from o/p stage



→ Amount of shift obtained is

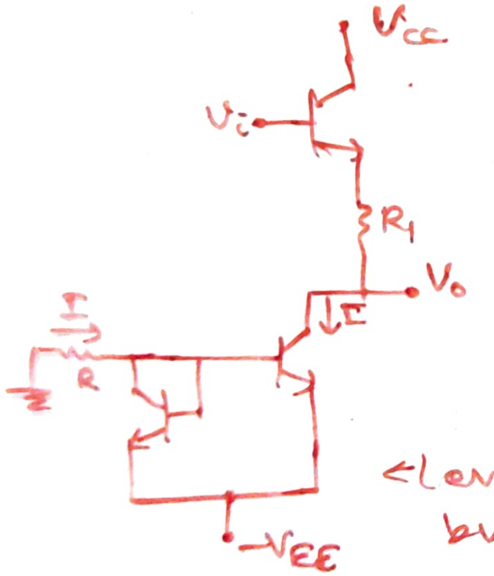
$V_o - V_i = -V_{BE} \simeq -0.7\ V$

→ If this shift is insufficient, the o/p can be taken at the junction of two resistors R_1 and R_2 as shown below.



→ Voltage shift is now increased by drop across R_1

→ Disadvantage in this arrangement is that signal voltage gets attenuated by $R_2/(R_1+R_2)$.



→ Shift in level is

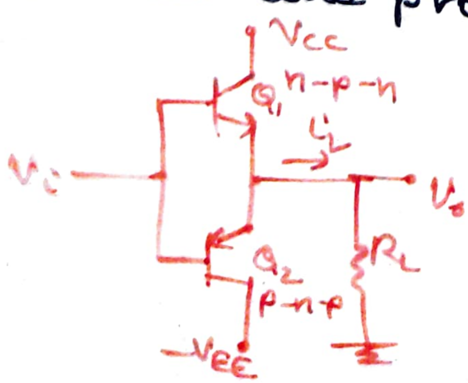
$V_o - V_i = -(V_{BE} + IR_1)$

& there is no ac attenuation due to high resistance of the current source

← Level shifters using emitter follower buffer

Output Stage

→ The function of o/p stage is to supply the load current and provide a low impedance o/p.



Complentary emitter follower o/p stage

→ If V_i is positive, Q_1 ON and supplies current to load R_L.

→ If V_i is negative, Q_1 is cut off & Q_2 acts a sink to remove current from load R_L.