Clock Skew and Time Race

→ In many digital circuits, the output of one flip-flop is connected either directly or through logic gates to the input of another flip-flop, and both flip-flops are triggered by the same clock signal.

→ The propogation delay of a flip-flop and/or the delays of the intervening gates make it difficult to predict precisely when the changing state of one flip-flop will be experienced at the input of another.

→ The clock signal which is applied simultaneously to all the flip-flops in a synchronous system may undergo varying degrees of delay caused by wiring between components, and arrive at the clk inputs of different flip-flops at different times. This delay is called clock skew.

→ If the clock skew is minimal, a flip-flop may get clocked before it receives a new input (derived from the output of another clocked flip-flop).

→ If the clock pulse is delayed significantly, the inputs to a flip-flop may have changed before the clock pulse arrives.

→ In these situations, we have a kind of a race between the two competing signals that are attempting to accomplish opposite effects. This can be termed time race.

→ The winner in such a race depends largely on unpredictable propogation delays.

→ The reliable systems operation is not possible when the responses of a flip-flop depend on the outcome of a race.