* Adders:

- Most basic arithmetic operation is the addition of two binary digits.

- Binary Addition: ↓ 4 possible operations →
  - $0+0=0$
  - $0+1=1$
  - $1+0=1$
  - $1+1=10$, with carry 1

- Adders are of 2 types: Half-Adder & Full Adder

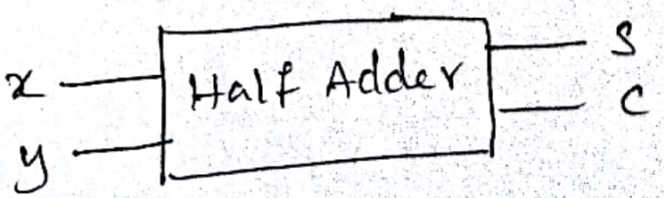
Half-Adder:

- Half adder is a combinational ckt ~~use~~ that performs the addition of two bits.

Step 1: No. of i/ps = 2 — x, y

No. of o/ps = 2 — S, C (S ↓ sum, C → carry)

Step 2: Truth table



x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

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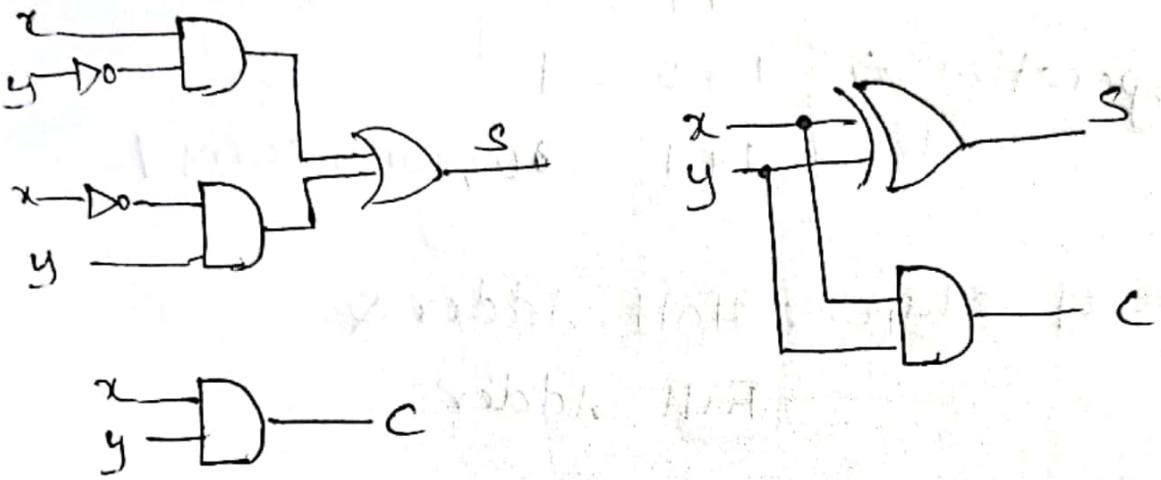
Step 3: Boolean expressions

$$S = xy' + x'y = x \oplus y$$

$$C = xy$$

Step 4: Logic diagram



Full Adder:

- Full adder is a combinational circuit that performs the addition of three bits (two significant bits and previous carry).

Step 1: No. of i/ps = 3 ; x, y, Z (or) A, B, Cin

No. of o/ps = 2 ; S, C

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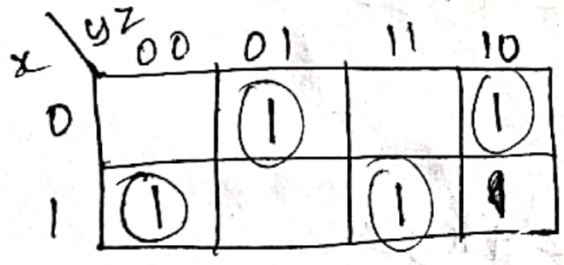
Step 2: Truth Table

Inputs			sum	carry
x	y	z	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Step 3: Boolean expressions

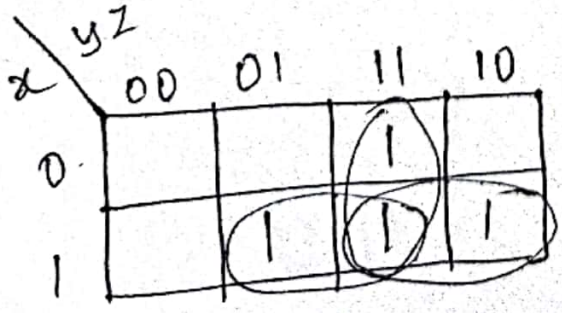
K-Map 3 variable



K-Map for s

$$s = x'y'z + x'yz' + xy'z' + xyz$$

$$= x \oplus y \oplus z$$



K-Map for c

$$c = yz + xz + xy$$

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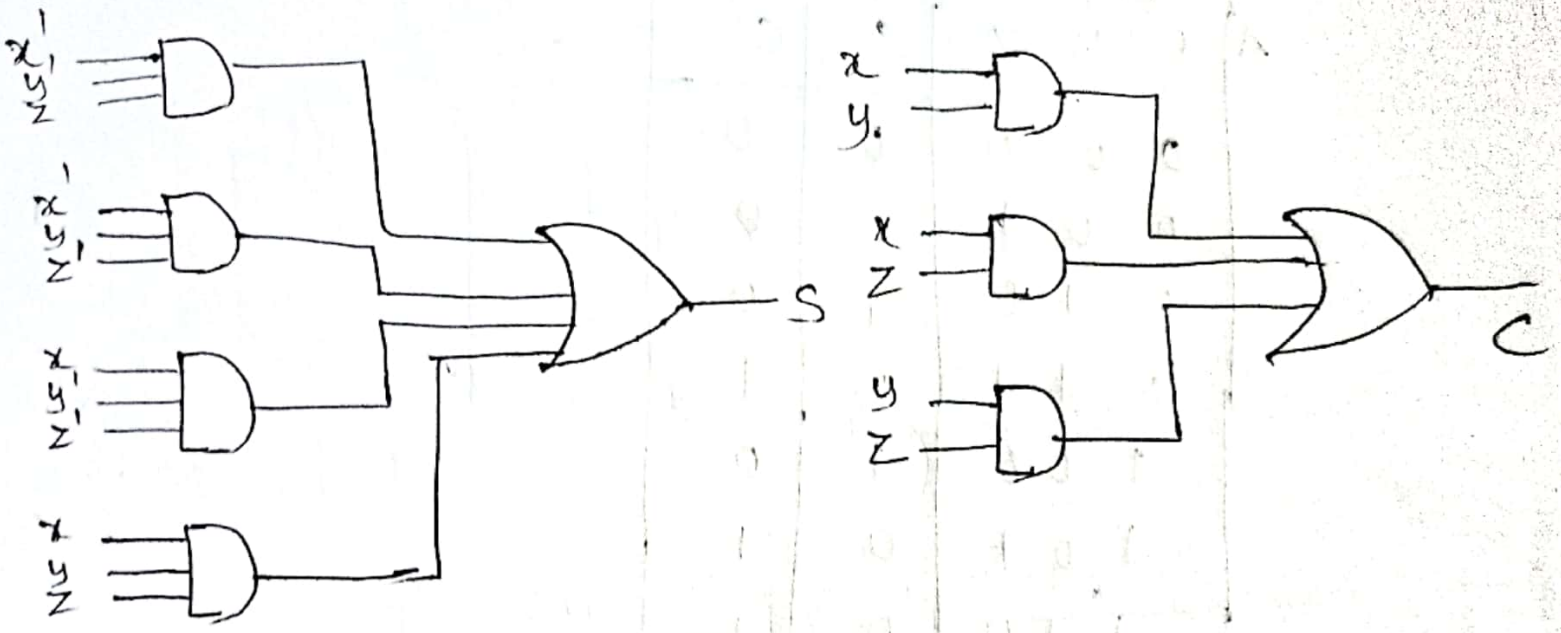
Step 4: logic diagram



Implementation of Full Adder using Half Adder:

WKT For full adder,

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$= x \oplus y \oplus z$$

$$C = x'yz + xy'z + xyz' + xyz$$

$$= z(x'y + xy') + xy(z + z')$$

$$= z(x \oplus y) + xy$$

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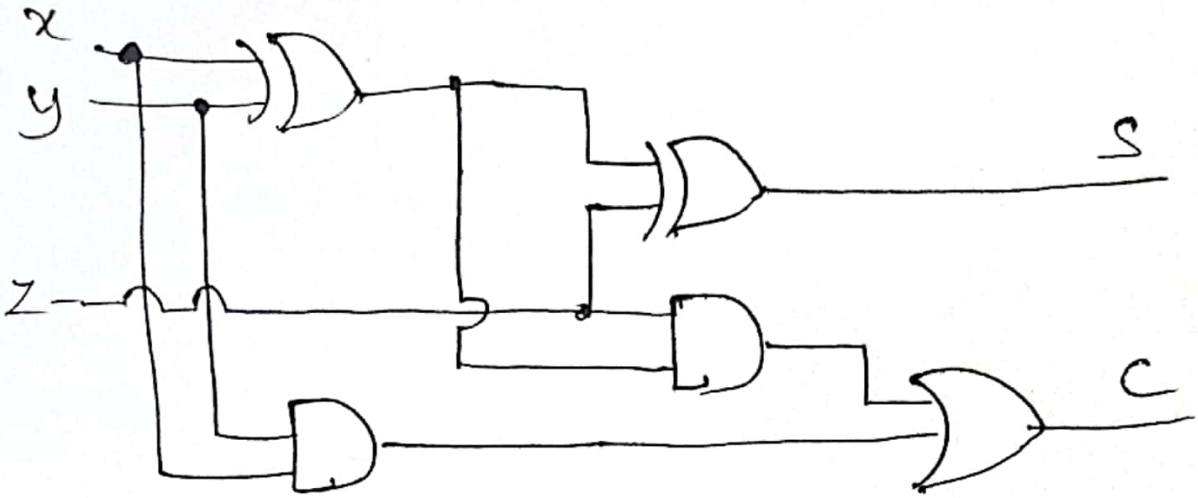

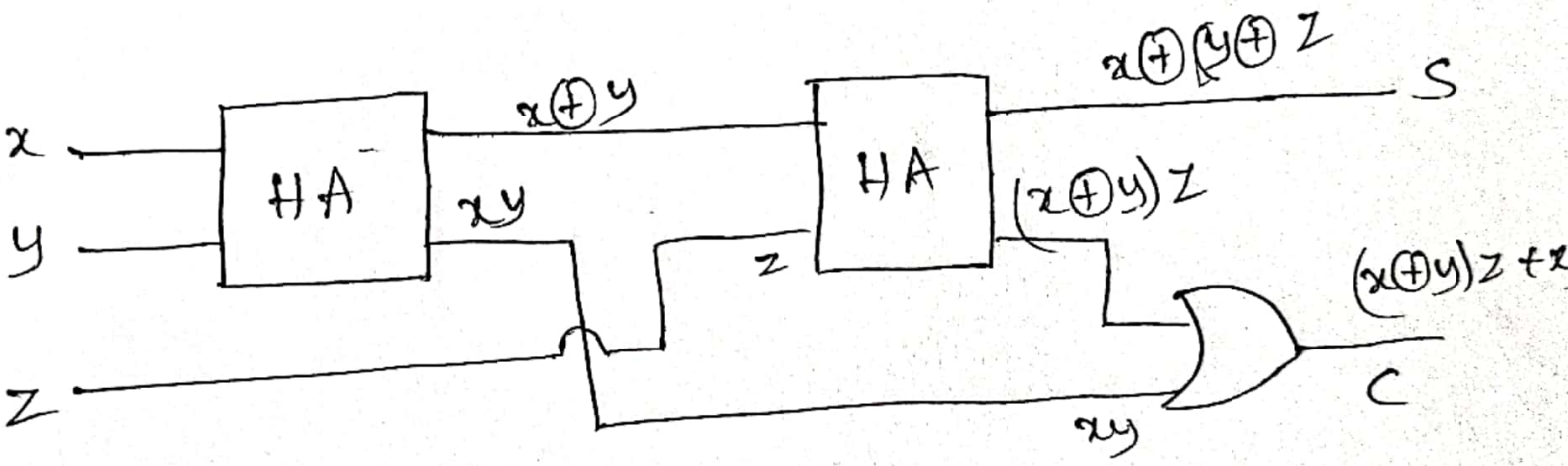

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A half-adder can also be realized in universal logic by using either only NAND gates or only NOR gates as shown in Figures 4.4 and 4.5 respectively.

NAND logic

$$S = A\bar{B} + \bar{A}B = A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$
$$= A \cdot \overline{AB} + B \cdot \overline{AB}$$
$$= \overline{A \cdot \overline{AB} \cdot B \cdot \overline{AB}}$$
$$C = AB = \overline{\overline{AB}}$$

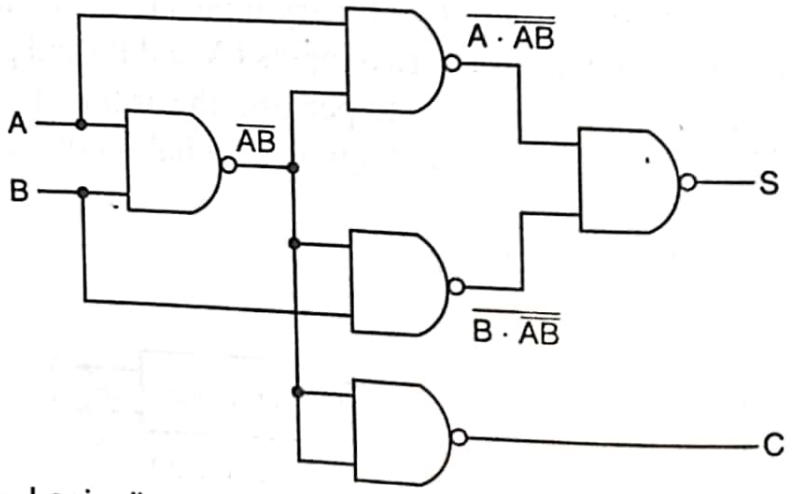

Figure 4.4 Logic diagram of a half-adder using only 2-input NAND gates.

NOR logic

$$S = A\bar{B} + \bar{A}B = A\bar{B} + A\bar{A} + \bar{A}B + B\bar{B}$$
$$= A(\bar{A} + \bar{B}) + B(\bar{A} + \bar{B})$$

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$$= (A + B)(\overline{A} + \overline{B})$$

$$= \overline{\overline{A + B} + \overline{\overline{A} + \overline{B}}}$$

$$C = AB = \overline{\overline{AB}} = \overline{\overline{A} + \overline{B}}$$

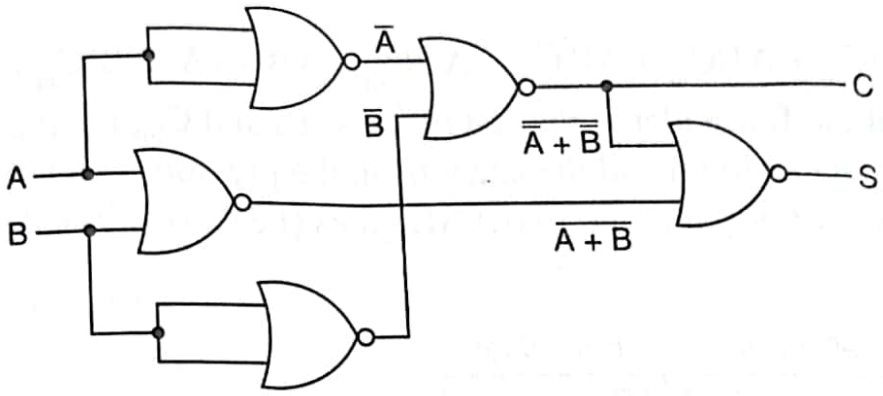

Figure 4.5 Logic diagram of a half-adder using only 2-input NOR gates.

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NAND logic

We know that

$$A \oplus B = \overline{\overline{A} \cdot \overline{AB} \cdot \overline{B} \cdot \overline{AB}}$$

Then

$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A \oplus B) \cdot \overline{(A \oplus B)C_{in}} \cdot \overline{C_{in}} \cdot \overline{(A \oplus B)C_{in}}}}$$

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$$C_{out} = C_{in}(A \oplus B) + AB = \overline{\overline{C_{in}(A \oplus B)} \cdot \overline{AB}}$$

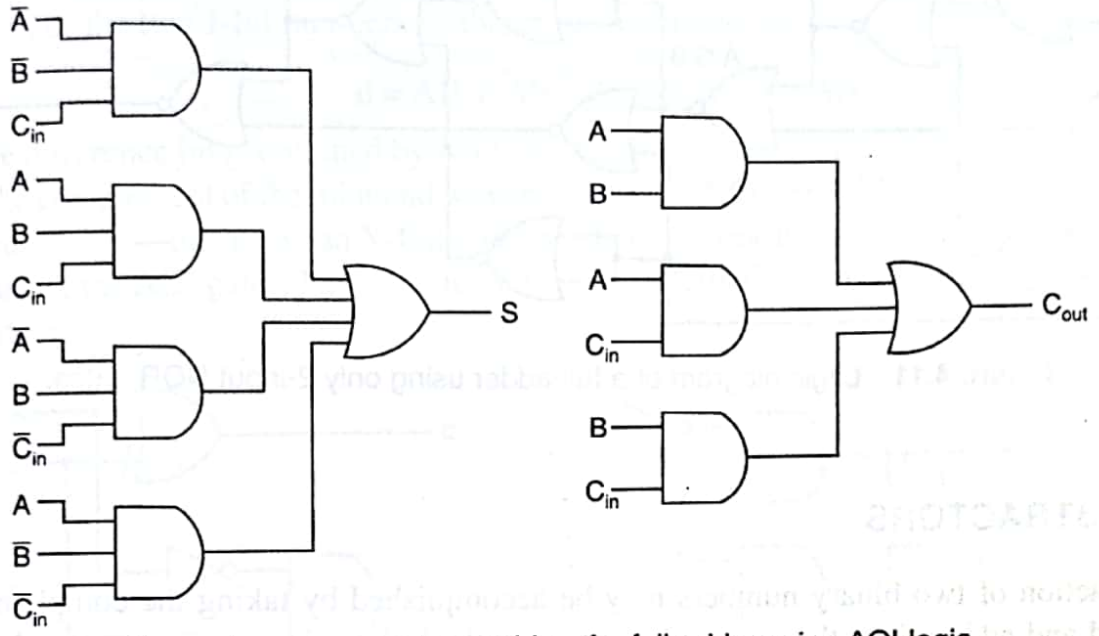

Figure 4.9 Sum and carry bits of a full-adder using AOI logic.

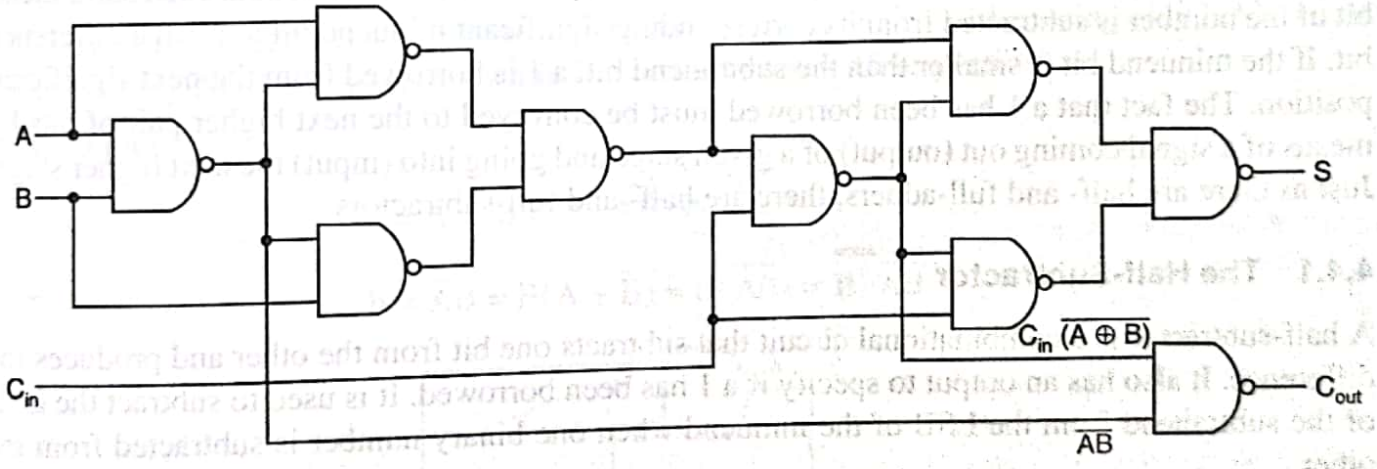

Figure 4.10 Logic diagram of a full-adder using only 2-input NAND gates.

NOR logic

We know that

$$A \oplus B = \overline{\overline{(A + B)} + \overline{\overline{A} + \overline{B}}}$$

Then

$$S = A \oplus B \oplus C_{in} = \overline{\overline{(A \oplus B) + \overline{C}_{in}} + \overline{\overline{(A \oplus B) + \overline{C}_{in}}}}$$

$$C_{out} = AB + C_{in}(A \oplus B) = \overline{\overline{A} + \overline{B}} + \overline{\overline{C}_{in} + \overline{A \oplus B}}$$

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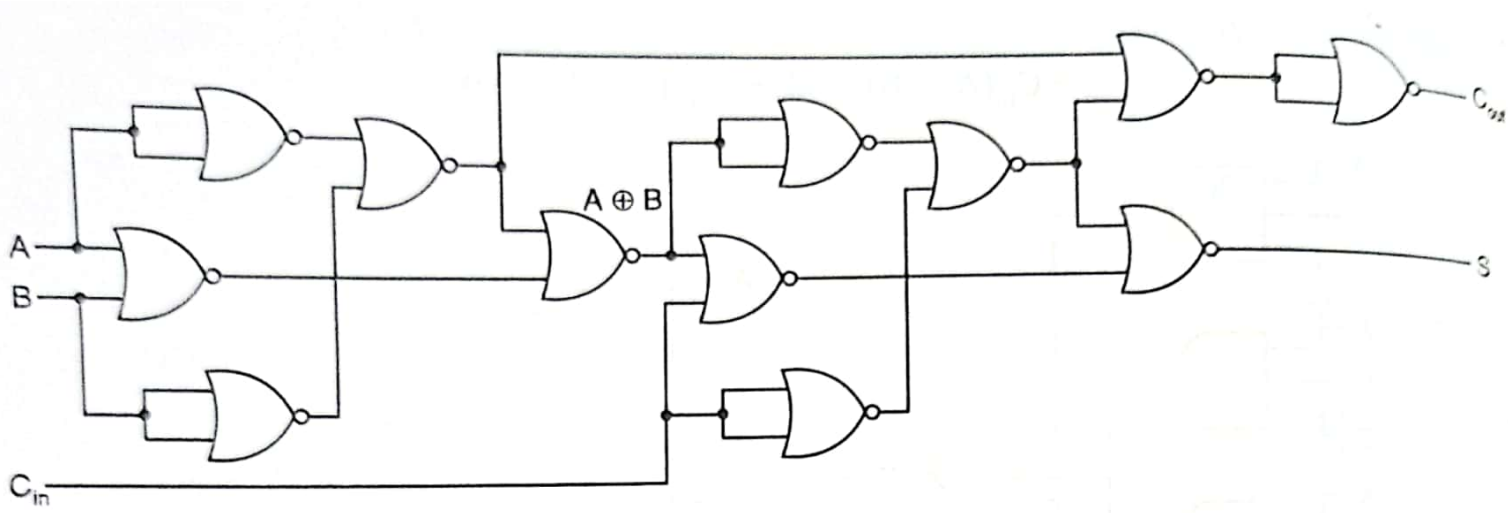

Figure 4.11 Logic diagram of a full-adder using only 2-input NOR gates.

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