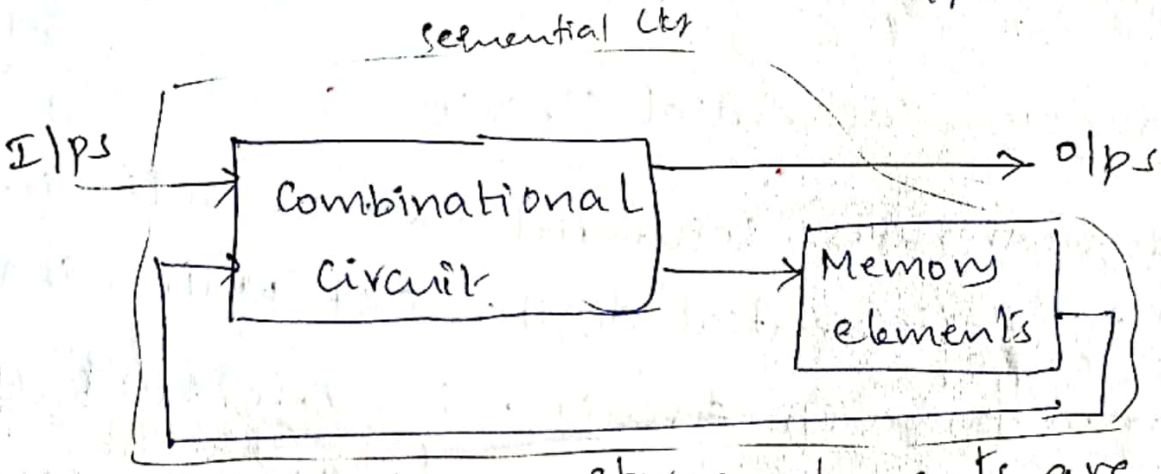
UNIT - III

* Sequential Circuits:

- Sequential circuits are combinational ckts with memory.
- In Sequential ckts, the present o/p depends on the present i/p as well as previous o/p (Present state)



- Memory elements are storage elements are connected to form a feed back path
- storage elements are devices capable of storing binary informations
- The information stored in sequential circuit represents present state
- The present state & present i/ps will define o/p & next state

Sequential ckts — 2 types — Synchronous
— asynchronous

Synchronous Sequential Circuits

- A synchronous circuit is a digital circuit in which the changes in the state of memory elements are synchronized by a clk signal
- Stored elements used in clked sequential ckts are called flip flops ~~& latches~~

Asynchronous Sequential Circuits

- An asynchronous sequential ckt or self-timed ckt is a sequential digital ckt which is not governed by a clk circuit. ie, the state of the device can change at any time in response to changing i/p's. Ex: latches

Latches:

- Latches are basic storage elements that operate with signal levels (rather than signal transitions). They are called level-sensitive devices
- 1-bit storage device
- unclked Flip flops

Combinational CKTs	Sequential CKTs
O/ps depends only on present i/ps	O/ps depend on both present i/ps & present state
F/b path is not present	F/b path is present
Memory elements are not required	Memory elements are required
Clock signal is not required	Clock signal is required
Easy to design	Difficult to design

* Definition of Flip-Flop:

- A flip-flop is the basic memory element used to store one bit of information
- It can store a 0 or a 1.
- The name flip-flop is because this circuit shifts back and forth b/w its two stable states upon application of proper i/ps.
- n-flip flops are required for storing n bits of information
- A flip-flop is known more formally as a bistable multivibrator. It has 2 stable states.

Applications of flip flops:

1. Used for data storage
2. a transfer of data
3. Counting
4. freq division
5. parallel-to-serial data converter
6. Serial-to-parallel data Converter

- Flip flops are edge-sensitive devices

* Definition of latch:

- An unclocked flip flop is called a latch.
- This name is because the o/p of the unclocked flip-flop latches onto a 1 or a 0 immediately after the i/p is applied
- A latch may be built by using two-cross coupled NOR gates or NAND gates.
- Latches are level-sensitive devices

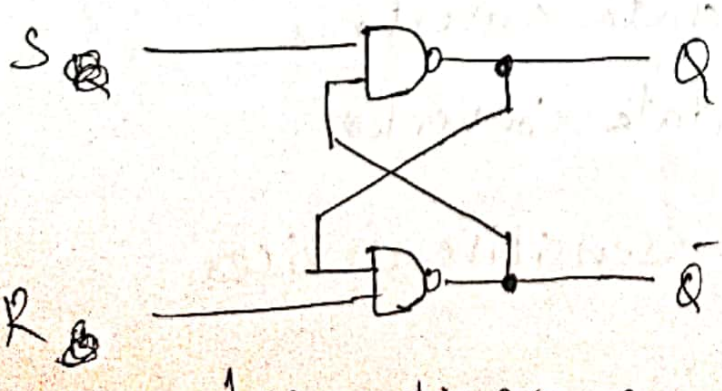
S-R Latch:

S → set

R → Reset

- The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two i/ps.

SR latch with NAND gates:



Logic diagram

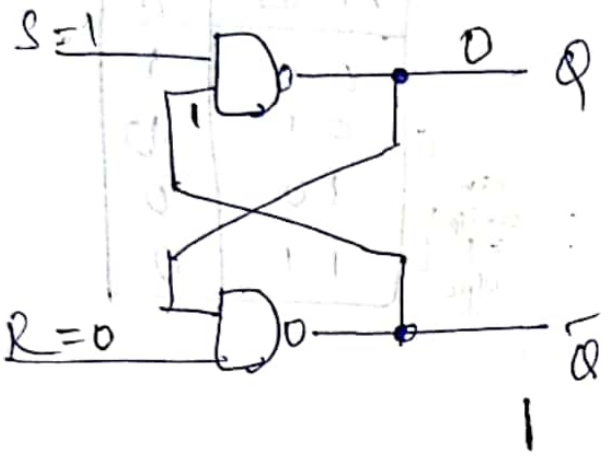
NAND

A B	o/p
0 0	1
0 1	1
1 0	1
1 1	0

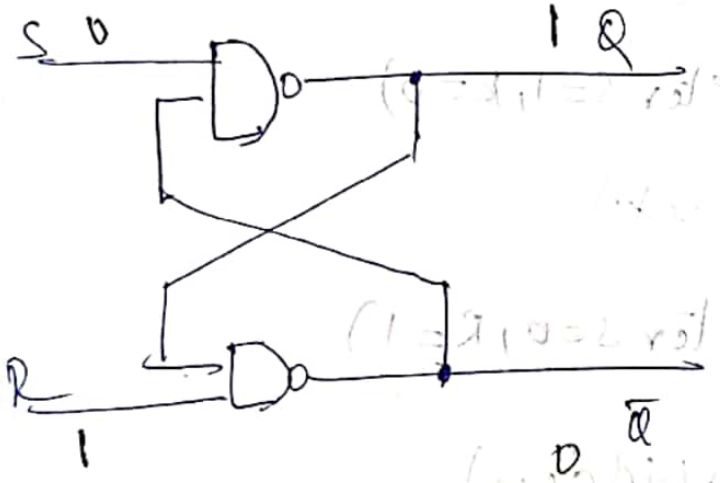
anyone i/p 0 to o/p → 1

Truth table

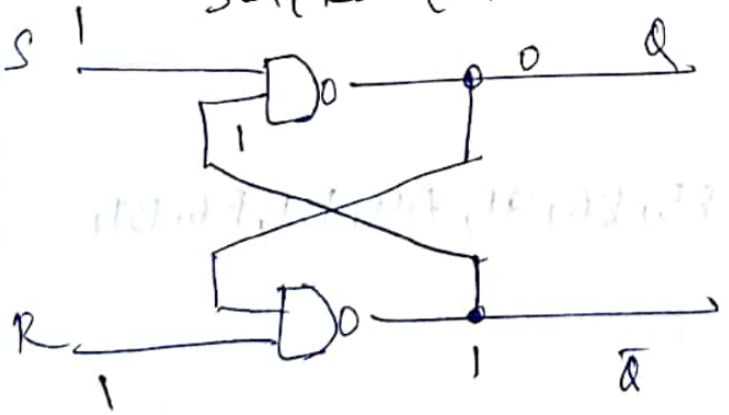
S=1, R=0



S=0, R=1

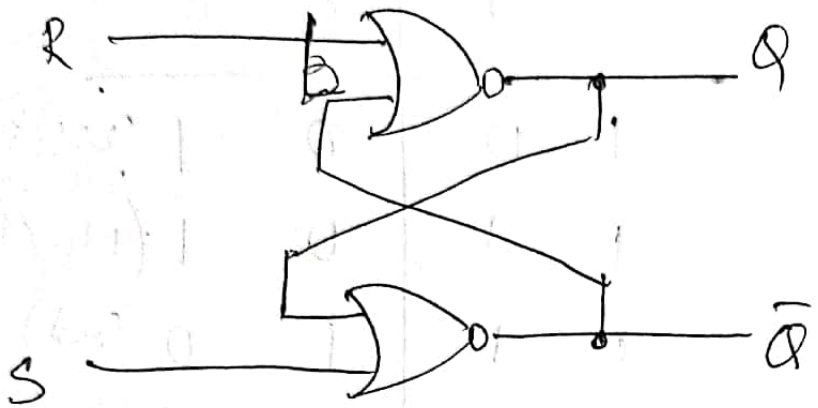


S=1, R=1 (after S=1, R=0)



S	R	Q	$\bar{Q}$	
1	0	0	1	(Reset) (after S=1, R=0)
1	1	0	1	(No Change)
0	1	1	0	(Set)
1	1	1	0	(after S=0, R=1 No change)
0	0	1	1	(forbidden)

S-R latch with NOR gates:



NOR TT

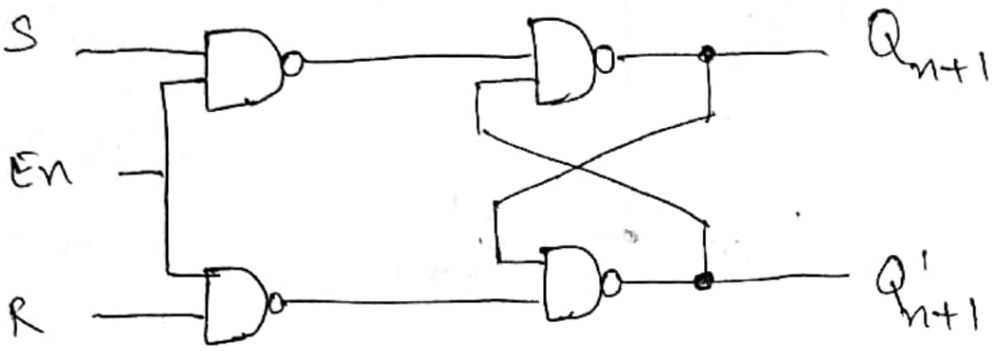
A	B	O/p
0	0	1
0	1	0
1	0	0
1	1	0

(any one i/p is 1 o/p 0)

S	R	Q	$\bar{Q}$	
1	0	1	0	(set)
0	0	1	0	(after S=1, R=0)
0	1	0	1	(Reset)
0	0	0	1	(after S=0, R=1)
1	1	0	0	(forbidden)

Latch	Flip flop
(1) Latch doesn't require clk signal	(1) Flip flop require clk signal
(2) level-sensitive device	(2) edge sensitive device
(3) Asynchronous device	(3) Synchronous device
(4) less power required	(4) More required
(5) Latch is based on enable signal	(5) ba based on clk signal

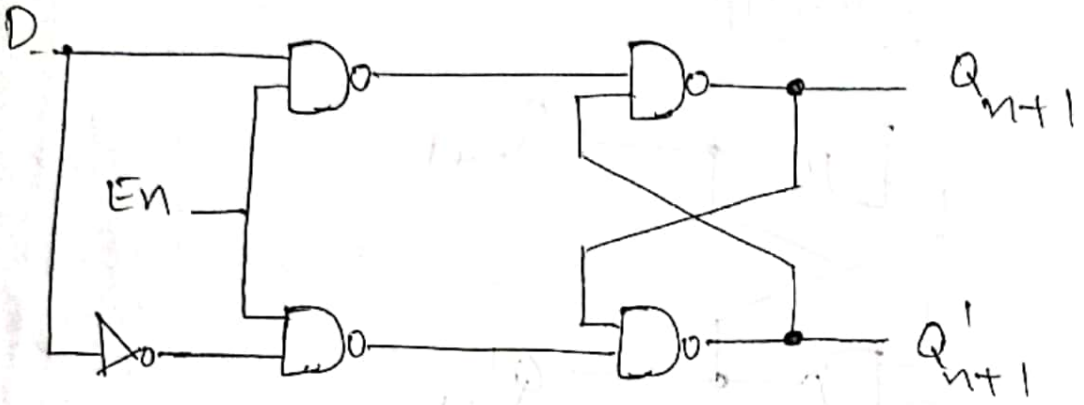
* SR latch with Enable i/p: or Control i/p OR SR Flip flop



En	S	R	Q'_{n+1} Q_{n+1}
0	X	X	No change Q_n Q'_n
1	0	0	Q_n Q'_n (No change)
1	0	1	0 1 (Reset)
1	1	0	1 0 (Set)
1	1	1	1 1 (indeterminate) (forbidden

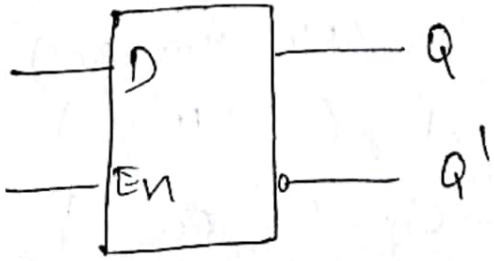
EN	S	R	Q_n	Q'_n	Q_{n+1}	Q'_{n+1}	
0	0	0	0	1	0	1	(No change)
			1	0	1	0	(No change)
0	0	1	0	1	0	1	(")
			1	0	1	0	(")
0	1	0	0	1	0	1	(")
			1	0	1	0	(")
0	1	1	0	1	0	1	(")
			1	0	1	0	(")

* D latch:



En	D	Q_{n+1}	Q'_{n+1}	
0	X	No change (Q_n)	(Q'_n)	
1	0	0	1	(Reset)
1	1	1	0	(Set)

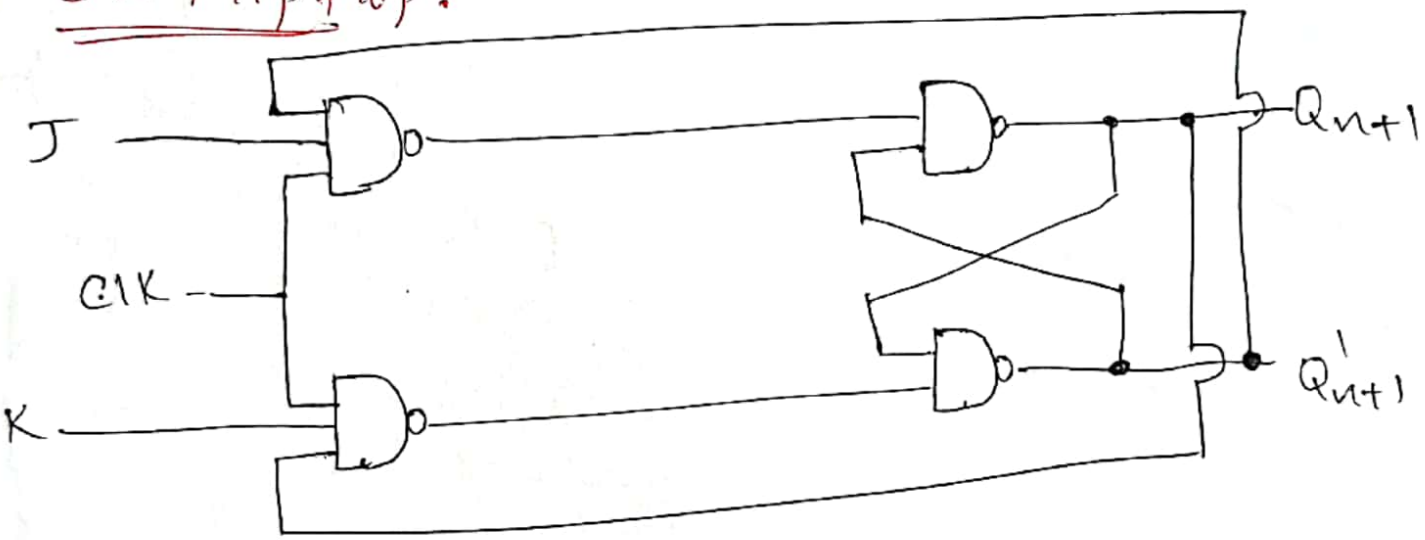
- when enable i/p is high, the o/p Q follows the i/p D ie; a low D i/p makes Q low (reset state) and a high D i/p makes Q high (set state). Therefore, a gated D latch is called a transparent latch



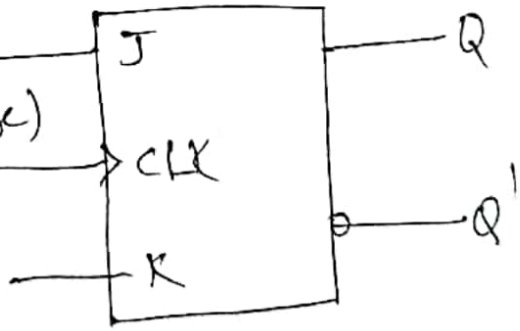
Drawback of SR FF:

The limitation with a S-R FF using NOR and NAND gate is the invalid state (undeterminate), when both i/ps are high at the clk pulse, it produces undesirable condition.

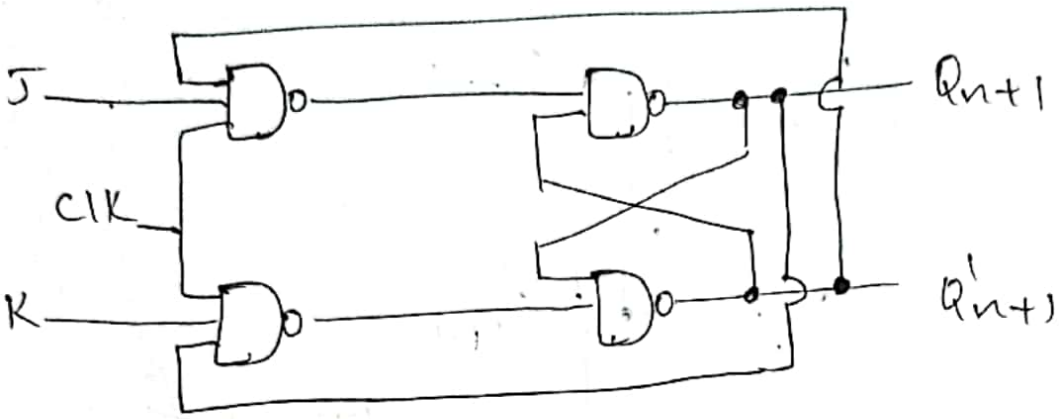
JK Flipflop:



CLK	J	K	Q_{n+1}	Q'_{n+1}
↑	0	0	Q_n	Q'_n (No change)
↑	0	1	0	1 (Reset)
↑	1	0	1	0 (Set)
↑	1	1	Q'_n	Q_n (Toggle)



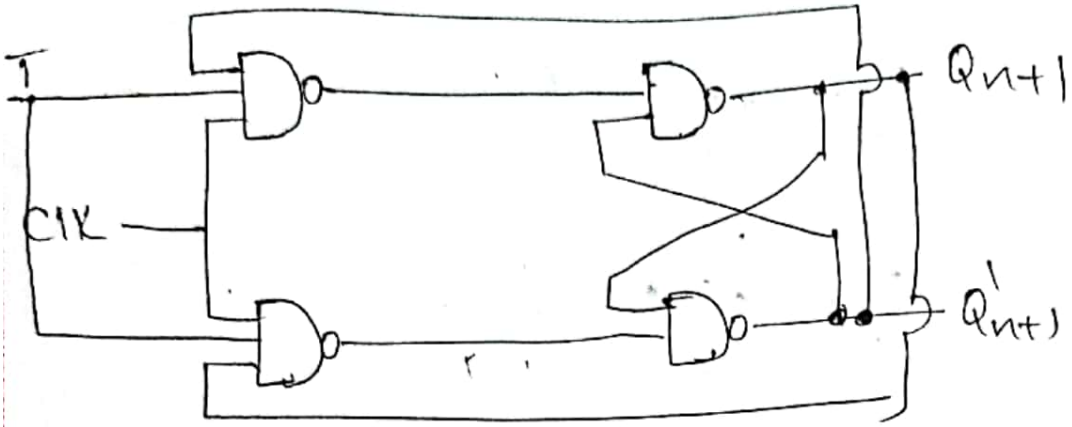
JK Flip Flop:



CLK	J	K	Qn	Q'n	Qn+1	Q'n+1	
↑	0	0	0	1	0	1	(No change)
			1	0	1	0	
↑	0	1	0	1	0	1	(Reset)
			1	0	0	1	
↑	1	0	0	1	1	0	(Set)
			1	0	1	0	
↑	1	1	0	1	1	0	(Toggle)
			1	0	0	1	

CLK	J	K	Qn+1	Q'n+1	
↑	0	0	Qn	Q'n	(No change)
↑	0	1	0	1	(Reset)
↑	1	0	1	0	(Set)
↑	1	1	Q'n	Qn	(Toggle)
0	x	x	Qn	Q'n	(No change)

T Flip Flop:



CLK	T	Q_{n+1}	Q'_{n+1}	
↑	0	Q_n	Q'_n	(No change)
↑	1	Q'_n	Q_n	(Complement)

CLK	T	Q_n	Q'_n	Q_{n+1}	Q'_{n+1}	
↑	0	0	1	0	1	(No change)
↑	0	1	0	1	0	(No change)
↑	1	0	1	1	0	(Complement)
↑	1	1	0	0	1	(Complement)