Decoders

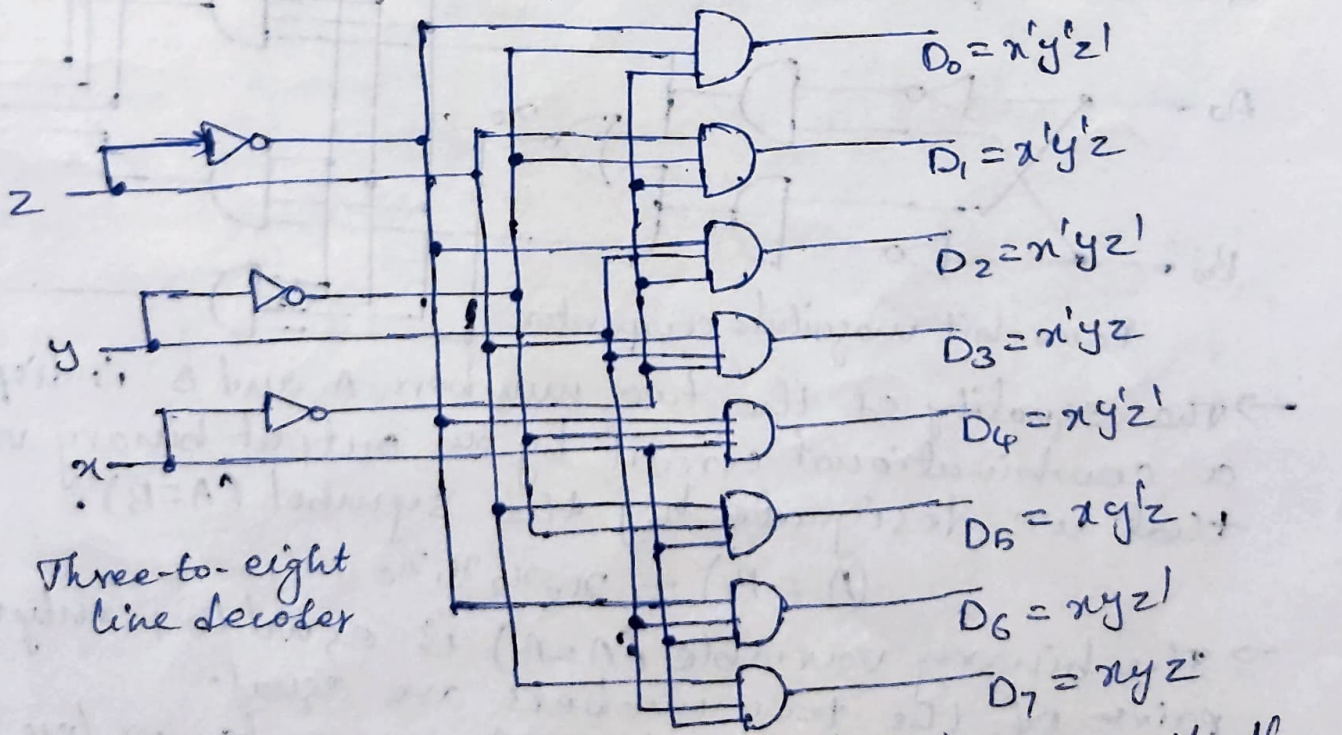
→ A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

→ If the n-bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.

→ The decoders are called n-to-m-line decoders, where $m \leq 2^n$

→ Their purpose is to generate the 2^n (or fewer) minterms of n input variables

→ Each combination of inputs will have a unique output



Three-to-eight line decoder

→ Consider the three-to-eight line decoder circuit, the three inputs are decoded into eight outputs, each representing one of the minterms of the three input variables.

→ The three inverters provide the complement of the inputs, and each one of the eight AND gates generates one of the minterms.

→ A particular application of this decoder is binary-to-octal conversion. The input variables represent a binary number, and the outputs represent the eight digits of a number in the octal number system.

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

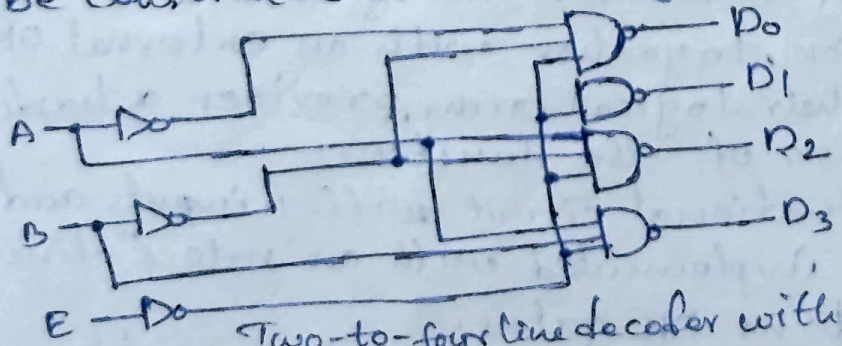
→ The operation of the decoder may be clarified by the truth table.

→ Some decoders are constructed with NAND gates.

→ Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form.

→ Decoders include one or more enable inputs to control the circuit operation.

→ A two-to-four line decoder with an enable input can be constructed with NAND gates.



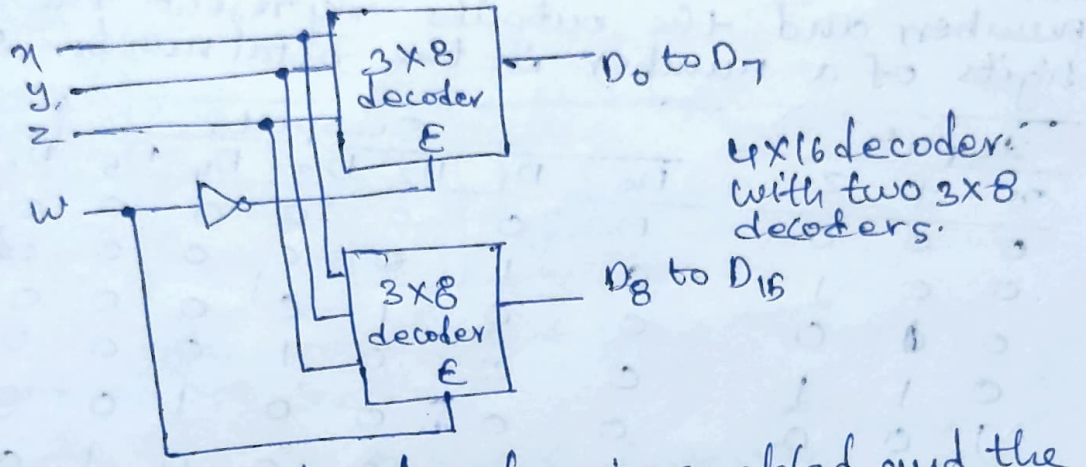
E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Two-to-four line decoder with enable input

→ The circuit operates with complemented outputs and a complement enable input.

→ The decoder is enabled when E is equal to 0 (i.e., active-low enable)

→ Decoders with enable inputs can be connected together to form a larger decoder circuit.
→ Two 3-to-8-line decoders with enable inputs can be connected to form a 4-to-16 line decoder



→ When w=0, the top decoder is enabled and the other is disabled.
→ The bottom decoder outputs are all 0's and the top eight outputs generate minterms 0000 to 0111
→ When w=1, the enable conditions are reversed.
→ The bottom decoder outputs generate minterms 1000 to 1111, while the outputs of the top decoder are all 0's.

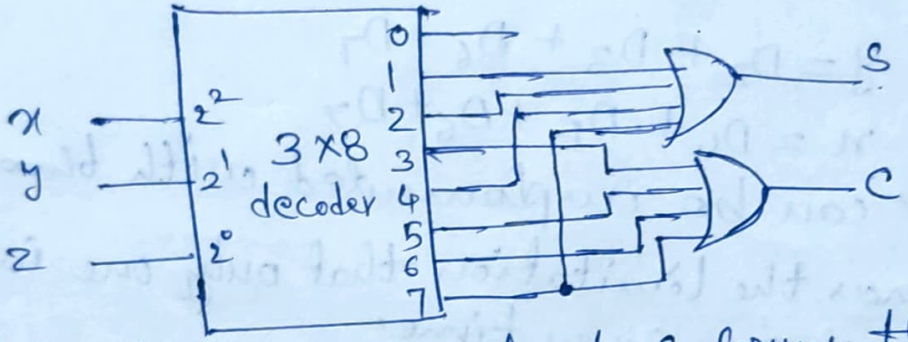
Combinational logic Implementation.

→ A decoder provides the 2^n minterms of n input variables.
→ Each output of the decoder is associated with a unique pattern of output bits.
→ Since any Boolean function can be expressed in sum-of-minterms form, a decoder that generates the minterms of the function, together with an external OR gate that forms their logical sum, provides a hardware implementation of the function.
→ So any combinational circuit with n inputs and m outputs can be implemented with an n-to-2^n-line decoder and m OR gates.
→ The procedure for implementing a full adder circuit with decoder is as follows:
↳ From the truth table, we obtain the functions for the combinational circuit in sum-of-minterms form:

$$S(x,y,z) = \sum(1,2,4,7) \; ; \; C(x,y,z) = \sum(3,5,6,7)$$

↳ Since there are three inputs and a total of eight minterms, we need a three-to-eight line decoder.

↳ The decoder generates the eight minterms of x, y and z



↳ The OR gate for output S forms the logical sum of minterms 1, 2, 4, and 7

↳ The OR gate for output C forms the logical sum of minterms 3, 5, 6, and 7