Encoders

→ An encoder is a digital circuit that performs the inverse operation of a decoder.

→ An encoder has 2^n (or fewer) input lines and n output lines

→ The output lines, as an aggregate, generate the binary code corresponding to the input value.

→ An example of an encoder is the octal-to-binary encoder which has eight inputs (one for each of the octal digits) and three outputs that generate the corresponding binary number.

→ It is assumed that only one input has a value of 1 at any given time

→ The encoder can be implemented with OR gates whose inputs are determined directly from the truth table

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

→ Output z is equal to 1 when the input octal digit is 1, 3, 5, or 7.
→ Output y is equal to 1 for the octal digits 2, 3, 6, or 7, and output x is 1 for digits 4, 5, 6, or 7

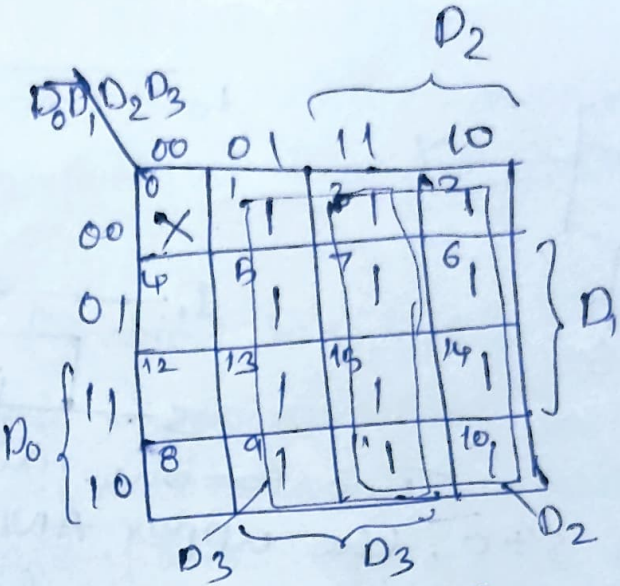
$$z = D_1 + D_3 + D_5 + D_7$$
$$y = D_2 + D_3 + D_6 + D_7$$
$$x = D_4 + D_5 + D_6 + D_7$$

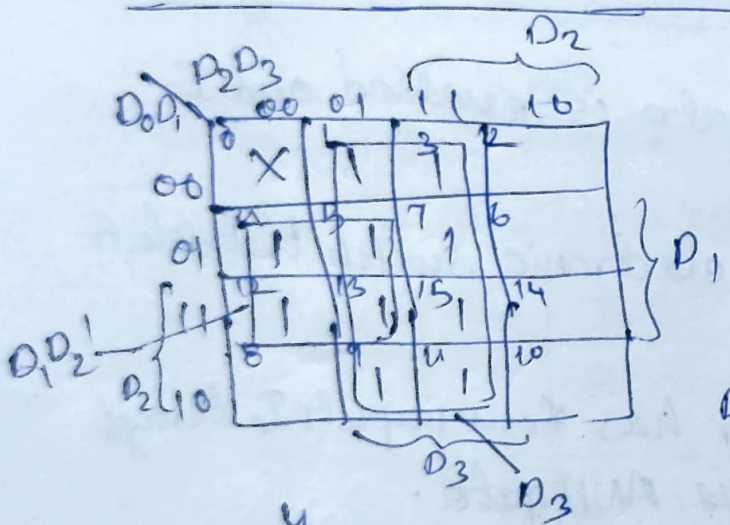
→ The encoder can be implemented with three OR gates.
→ The encoder has the limitation that only one input can be active at any given time.
→ If two inputs are active simultaneously, the output produces an undefined combination.
→ To resolve this ambiguity, encoder circuits must establish an input priority to ensure that only one input is encoded.
→ Another ambiguity in the octal-to-binary encoder is that an output with all 0's is generated when all the inputs are 0; but this output is same as when D_0 is equal to 1
→ This discrepancy can be resolved by providing one more output to indicate whether at least one input is equal to 1

Priority Encoder

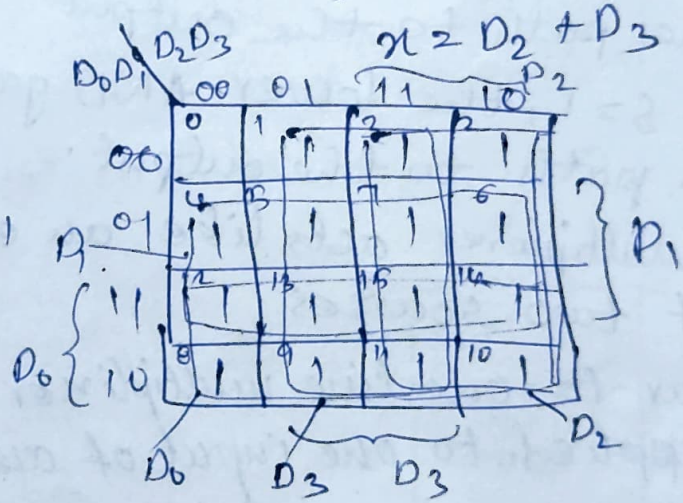
→ A priority encoder is an encoder circuit that includes the priority function.
→ The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time the input having the highest priority will take precedence.
→ In addition to the two outputs x and y, the circuit has a third output designated by V; this is a valid bit indicator that is set to 1 when one or more inputs are equal to 1
→ If all inputs are 0, there is no valid input and V is equal to 0
→ The other two outputs are not inspected when V equals 0 and are specified as don't-care conditions.

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

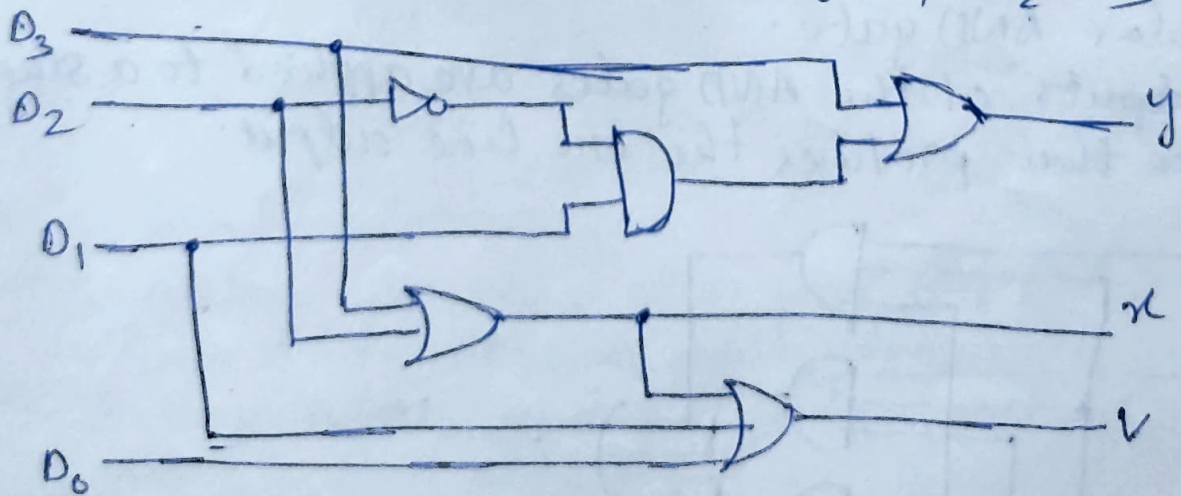




$y = D_3 + D_1 D_2'$



$V = D_0 + D_1 + D_2 + D_3$



Four-bit priority encoder