Storage Elements: Flip-flops

→ The state of a latch or flip-flop is switched by a change in the control input. This momentary change is called a trigger, and the transition it causes is said to trigger the flip-flop.

→ The D latch with pulses in its control input is essentially a flip-flop that is triggered every time the pulse goes to the logic-1 level.

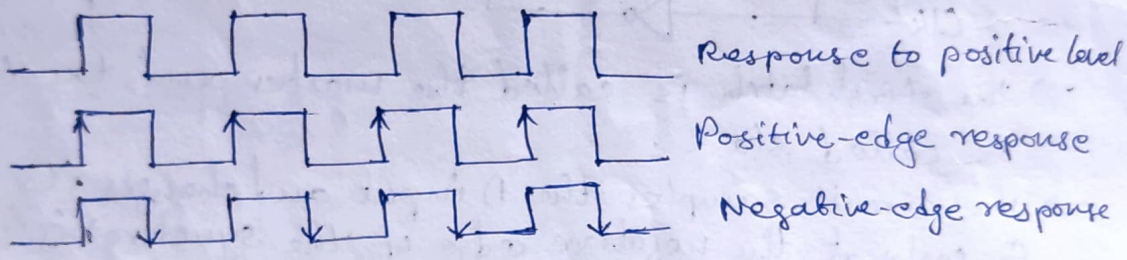
→ As long as the pulse input remains at this level, any changes in the data input will change the output and the state of the latch.

→ When latches are used for the storage elements, a serious difficulty arises.

→ The state transitions of the latches start as soon as the clock pulse changes to the logic-1 level.

→ The new state of a latch appears at the output while the pulse is still active.

→ This output is connected to the inputs of the latches through the combinational circuit.
→ If the inputs applied to the latches change while the clock pulse is still at the logic-1 level, the latches will respond to new values and a new output state may occer.
→ The result is an unpredictable situation, since the state of the latches may keep changing for as long as the clock pulse stays at the active level.
→ Because of this unreliable operation, the output of a latch cannot be applied directly or through combinational logic to the input of the same or another latch when all the latches are triggered by a common clock source.
→ Flip-flop circuits are constructed in such a way as to make them operate properly when they are part of a sequential circuit that employs a common clock.



Clock response in latch and flip-flop

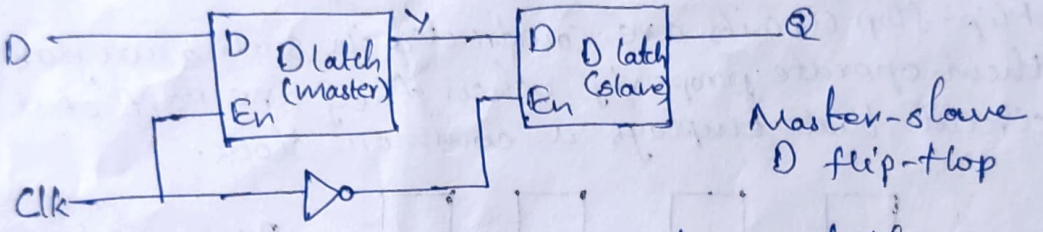
→ The problem with the latch is that it responds to a change in the level of a clock pulse.
→ A positive level response in the enable input allows changes in the output when the D input changes while the clock pulse stays at Logic 1.
→ The key to the proper operation of a flip-flop is to trigger it only during a signal transition.
→ This can be accomplished by eliminating the feedback path that is inherent in the operation of the sequential circuit using latches.
→ A clock pulse goes through two transitions: from 0 to 1 and the return from 1 to 0.
→ The positive transition is defined as the positive edge and the negative transition as the negative edge.
→ There are two ways that a latch can be modified to form a flip-flop.

→ One way is to employ two latches in a special configuration that isolates the output of the flip-flop and prevents it from being affected while the input to the flip-flop is changing.

→ Another way is to produce a flip-flop that triggers only during a signal transition (from 0 to 1 or from 1 to 0) of the synchronizing signal (clock) and is disabled during the rest of the clock pulse.

Edge Triggered D Flip-Flop

→ The construction of a D flip-flop consists of two D latches and an inverter



Master-slave D flip-flop

→ The first latch is called the master and the second is called slave.

→ The circuit samples the D input and changes its output Q only at the negative edge of the synchronizing or controlling clock (designated as Clk).

→ When the clock is 0, the output of the inverter is 1. The slave latch is enabled, and its output Q is equal to the master output Y. The master latch is disabled because Clk=0.

→ When the input (clock) pulse changes to the logic-1 level, the data from the external D input are transferred to the master output Y.

→ However, the slave is disabled as long as the clock remains at the 1 level, because its enable input is equal to 0.

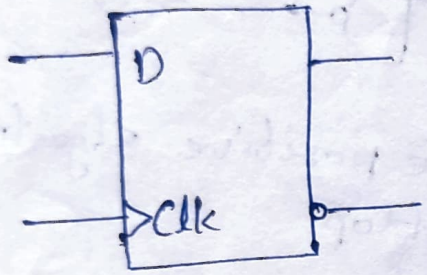
→ Any change in the input changes the master output at Y, but cannot affect the slave output.

→ When the clock pulse returns to 0, the master is disabled and is isolated from the D input. At the same time, the slave is enabled and the value of Y is transferred to the output of the flip-flop at Q.

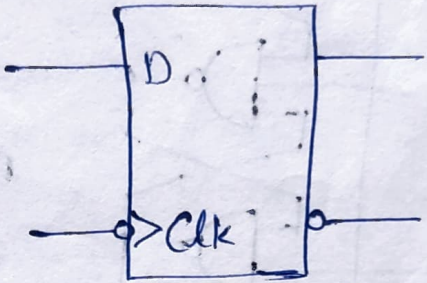
→ Thus, a change in the output of the flip-flop can be triggered only by and during the transition of the clock from 1 to 0.

→ The behavior of the master-slave flip-flop describes that
(1) the output may change only once,
(2) the change in the output is triggered by the negative edge of the clock, and
(3) the change may occur only during the clock's negative level.

→ The value that is produced at the output of the flip-flop is the value that was stored in the master stage immediately before the negative edge occured.



positive-edge



negative-edge

Graphic symbol for edge-triggered D flip-flop

→ The graphic symbol for the edge-triggered D flip-flop is similar to the symbol used for D latch, except for the arrowhead-like symbol in front of the letter Clk, designating a dynamic input.

→ The dynamic indicator (>) denotes that the flip-flop responds to the edge transition of the clock.

→ A bubble outside the block adjacent to the dynamic indicator designates a negative edge for triggering the circuit.

→ The absence of a bubble designates a positive-edge response.

Other Flip-Flops

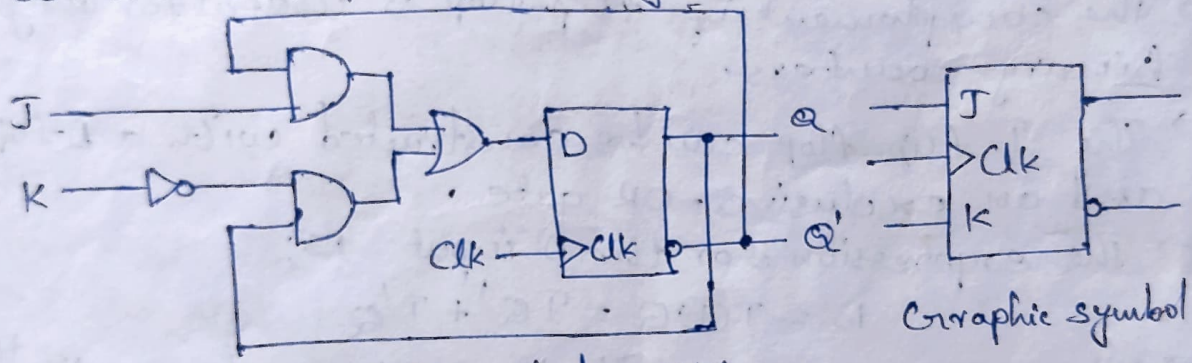
→ Each flip-flop is constructed from an interconnection of gates.

→ The most economical and efficient flip-flop constructed in this manner is the edge-triggered D flip-flop, because it requires smallest number of gates.

→ Other types of flip-flops can be constructed by using the D flip-flop and external logic.

→ Two flip-flops less widely used in the design of digital systems are the JK and T flip-flops.

→ The circuit diagram of a JK flip-flop constructed with a D flip-flop and gates.



Circuit diagram — Graphic symbol

JK flip-flop

→ The J input sets the flip-flop to 1, the K input resets it to 0, and when both inputs are enabled, the output is complemented.

→ This can be verified from the circuit applied to the D input: $D = JQ' + K'Q$.

→ When J=1 and K=0, $D = Q' + Q = 1$, so the next clock edge sets the output to 1.

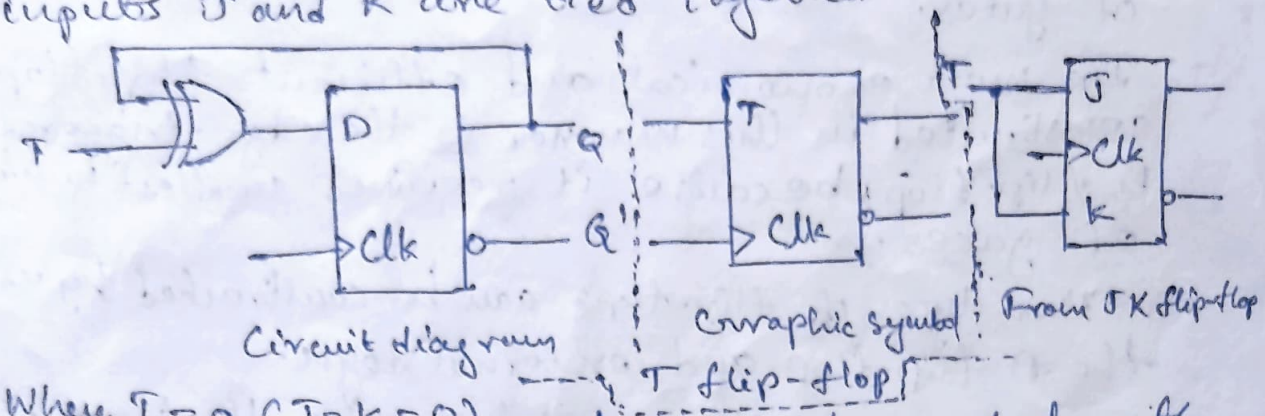
→ When J=0 and K=1, D=0, so the next clock edge resets the output to 0.

→ When both J=K=1 and $D = Q'$, the next clock edge complements the output.

→ When both J=K=0 and D=Q, the clock edge leaves the output unchanged.

→ The graphic symbol for the JK flip-flop is similar to that of the D flip-flop; except that the inputs are marked J and K.

→ The T (toggle) flip-flop is a complementing flip-flop and can be obtained from a JK flip-flop when inputs J and K are tied together.



→ When T=0 (J=K=0), a clock edge does not change the output.

→ When T=1 (J=K=1), a clock edge complements the output.

→ The complementing flip-flop is useful for designing Binary counters.

→ The T flip-flop can be constructed with a D-flip-flop and an exclusive-OR gate.

→ The expression for the D input is:

$$D = T \oplus Q = TQ' + T'Q$$

→ When T=0, D=Q and there is no change in the output.

→ When T=1, D=Q' and the output complements.

→ The graphic symbol for this flip-flop has a T symbol in the input.

Characteristic Tables

→ A characteristic table defines the logical properties of a flip-flop by describing its operation in tabular form.

→ They define the next state (i.e., the state that results from a clock transition) as a function of the inputs and the present state.

→ Q(t) refers to the present state (i.e., the state present before the application of a clock edge).

→ Q(t+1) is the next state one clock period later.

→ The clock edge input is not included in the characteristic table, but is implied to occur between times t and t+1.

JK Flip-flop		
J	K	Q(t+1)
0	0	Q(t) No change
0	1	0 Reset
1	0	1 Set
1	1	Q'(t) Complement

D Flip-flop	
D	Q(t+1)
0	0 Reset
1	1 Set

T Flip-flop	
T	Q(t+1)
0	Q(t) No change
1	Q'(t) Complement

SR Flip-flop		
S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	?

Q(t+1) = S + QR'

Characteristic Equations

→ The logical properties of a flip-flop, as described in the characteristic table, can be expressed algebraically with a characteristic equation.

→ For D flip-flop, $Q(t+1) = D$, which states that the next state of the output will be equal to the value of input D in the present state.

→ For JK flip-flop, $Q(t+1) = JQ' + K'Q$, where Q is the value of the flip-flop output before the application of a clock edge.

→ For T flip-flop, $Q(t+1) = T \oplus Q = TQ' + T'Q$