Storage Elements: Latches

→ A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.

→ The major differences among various types of storage elements are in the number of inputs they possess and in the manner in which the inputs affect the binary state.

→ Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches and those controlled by a clock transition are flip-flops.

→ Latches are said to be level sensitive devices whereas flip-flops are edge-sensitive devices.

→ Although latches are useful for storing binary information and for the design of asynchronous sequential circuits, they are not practical for use as storage elements in synchronous sequential circuits.

SR Latch

→ The SR latch is a circuit with two cross-coupled NOR gates or two cross-coupled NAND gates, and two inputs labeled S for set and R for reset.

→ The latch has two useful states.

→ When output $Q = 1$ and $Q' = 0$, the latch is said to be in set state.

→ When $Q = 0$ and $Q' = 1$, it is in reset state.

→ When both inputs are equal to 1 at the same time, a condition in which both outputs are equal to 0 occurs.

→ If both inputs are then switched to 0 simultaneously, the device will enter an unpredictable or undefined state or a metastable state.

→ So in practical applications setting both inputs to 1 is forbidden.

→ Under normal conditions, both inputs of the latch remain at 0 unless the state has to be changed.

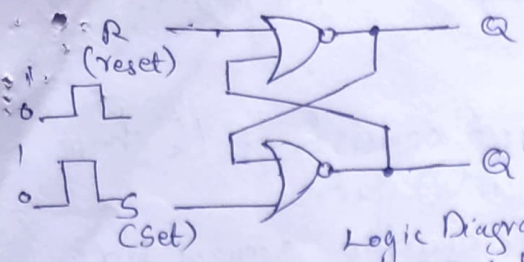
→ The application of a momentary 1 to the S input causes the latch to go to the set state.

→ Removing the active input from S leaves the circuit in the same state.

→ After both inputs return to 0, it is then possible to shift to the reset state by momentary applying a 1 to the R input.

→ The 1 can then be removed from R, whereupon the circuit remains in the reset state.

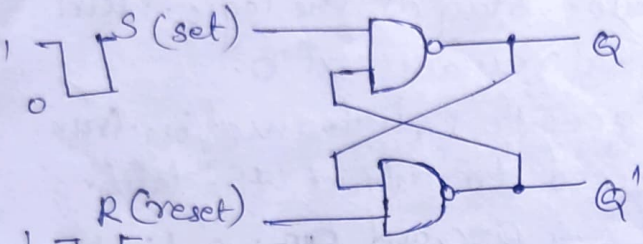
→ If a 1 is applied to both the S and R inputs of latch, both outputs go to 0. This action produces an undefined next state.



Logic Diagram of SR latch with NOR gates

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after S=1, R=0)
0	1	0	1	
0	0	0	1	(after S=0, R=1)
1	1	0	0	(forbidden)

Function Table



Logic Diagram of SR latch with NAND gates

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after S=1, R=0)
0	1	1	0	
1	1	1	0	(after S=0, R=1)
0	0	1	1	(forbidden)

Function Table

→ The SR latch with two cross-coupled NAND gates operates with both inputs normally at 1, unless the state of the latch has to be changed.

→ The application of 0 to the S input causes output Q to go to 1, putting the latch in the set state.

→ When the S input goes back to 1, the circuit remains in set state

→ After both inputs go back to 1, to change the state of the latch by placing a 0 in the R input, causes the circuit to go to the reset state and stay even after both inputs being equal to 0 at the same time, an input combination that should be avoided.

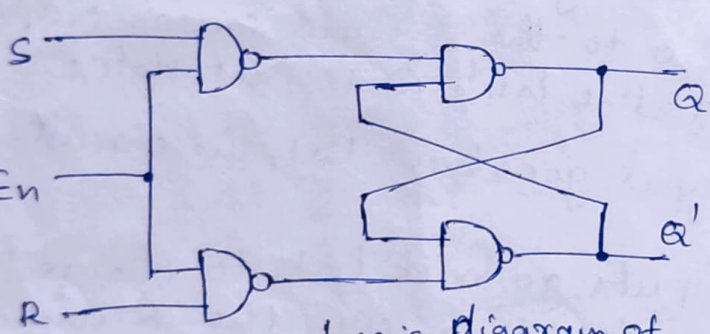
→ In comparing the NAND with the NOR latch, the input signals for NAND require the complement of those values used for the NOR latch.

→ Beause the NAND latch requires a 0 signal to change its state, so it is sometimes referred to as an S'R' latch.

→ The operation of the basic SR latch can be modified by providing an additional input signal that determines (controls) when the state of the latch can be

can be changed by determining whether S and R (or S' and R') can affect the circuit.

→ An SR-latch with a control input consists of the basic SR latch and two additional NAND gates.
→ The control input En acts as an enable signal for the other two inputs.
→ The outputs of the NAND gates stay at the logic-1 level as long as the enable signal remains at 0.
→ When the enable input goes to 1, information from the S or R input is allowed to affect the latch.
→ The set state is reached with S=1, R=0 and En=1 (active-high enabled).
→ To change to the reset state, the inputs must be S=0, R=1, and En=1.
→ In either case, when En returns to 0, the circuit remains in its current state.



Logic diagram of SR Latch with control input

En	S	R	Next state of Q
0	x	x	No change
1	0	0	No change
1	0	1	Q=0; reset state
1	1	0	Q=1, set state
1	1	1	Indeterminate

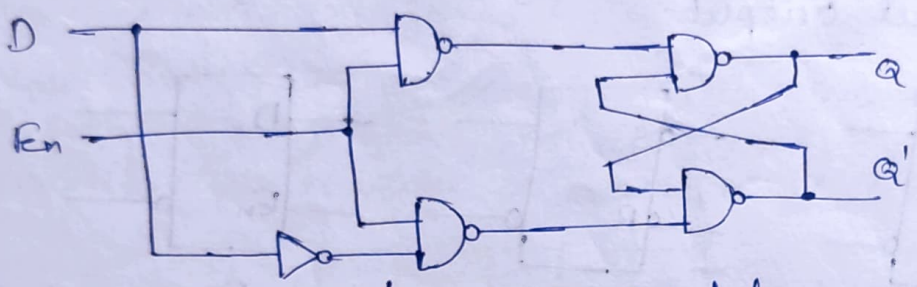
Function table

→ The control input disables the circuit by applying 0 to En, so that the state of the output does not change regardless of the values of S and R.
→ When En=1 and both the S and R inputs are equal to 0, the state of the circuit does not change.
→ An indeterminate condition occurs when all three inputs are equal to 1. This condition places 0's on both inputs of the basic SR latch, which puts it in undefined state.
→ When the enable input goes back to 0, one cannot determine the next state, because it depends on whether the S or R input goes to 0 first.

→ This indeterminate condition makes this circuit difficult to manage, and it is rarely used in practice.
→ But the SR latch is an important circuit because other useful latches and flip-flops are constructed from it.

D latch (Transparent latch)

→ One way to eliminate the undesirable condition of the indeterminate state in SR latch is to ensure that inputs S and R are never equal to 1.
→ This is done in the D latch



Logic diagram of D latch

En	D	Next state of Q
0	X	No change
1	0	Q=0; reset state
1	1	Q=1; set state

Function table

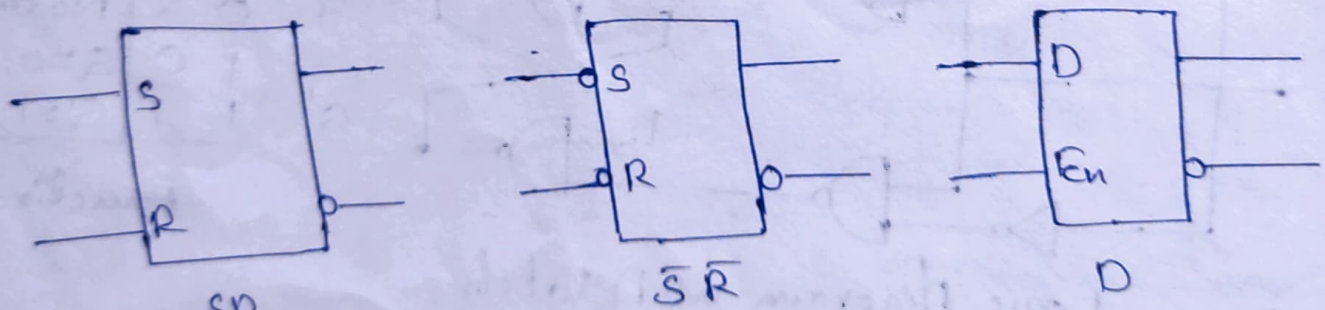
→ This latch has only two inputs: D (data) and En (enable)
→ The D input goes directly to the S input, and its complement is applied to the R input.
→ As long as the enable input is at 0, the cross-coupled SR latch has both inputs at the 1 level and the circuit cannot change state regardless of the value of D
→ The D input is enabled when En = 1.
→ If D = 1, the Q output goes to 1, placing the circuit in the set state.
→ If D = 0, output Q goes to 0, placing the circuit in the reset state.
→ The D latch receives that name from its ability to hold data in its internal storage.
→ It is suited for use as a temporary storage for binary information between a unit and its environment.
→ The binary information present at the data input of the D latch is transferred to the Q output when the enable input is set (1).

→ This provides a path from input D to the output, and for this reason, the circuit is often called a transparent latch.

→ When the enable input signal is reset (0), the binary information that was present at the data input at the time the transition occured is retained (i.e., stored) at the Q output until the enable input is set (1) again.

→ The graphic symbols of a latch is designated by a rectangular block with inputs on the left and outputs on the right.

→ One output designates the normal output, and the other (with the bubble designation) designates the complement output.



Graphic symbols for latches