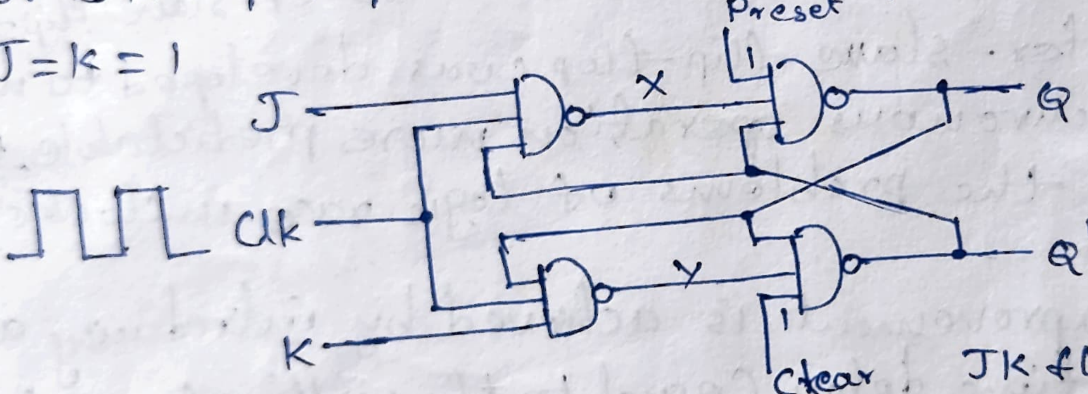
Race Around Condition

→ For JK flip-flop consider the assignment of excitations
$J = K = 1$



JK flip-flop using NAND gate

→ If the width of the clock pulse t_p is too long, the state of the flip-flop will keep on changing from 0 to 1, 1 to 0, 0 to 1 and so on, and at the end of the clock pulse, its state will be uncertain. This phenomenon is called race around condition.

→ The outputs Q and Q' will change on their own if the clock pulse width t_p is too long compared with the propogation delay τ of each NAND gate.

→ Assuming that the clock pulse occurs at $t=0$, and $t_p >> T$, the following tables shows how Q and Q' keep on changing with time.

	Time	X	Y	Q	Q'
Initial	$t<0$	1	1	0	1
$t \geq 0$	$t=T$	0	1	0	1
	$t=2T$	0	1	1	1
	$t=3T$	0	0	1	0
	$t=4T$	1	0	1	1
	$t=5T$	0	0	0	1
	$t=6T$	0	1	1	1
	$t=7T$	0	0	1	0
	$t=8T$	1	0	1	1

→ Thus the state of the flip-flop keeps on complementing itself for every 2T.

→ The clock pulse width should be such as to allow only the change to complement the state and not too long to allow many changes resulting in uncertainity about the final state.

→ The race around problem is eliminated using master-slave flip-flop or edge triggered flip-flop.

Master-Slave (Pulse-Triggered) Flipflops

→ Before the development of edge-triggered flip-flops the timing problems were often handled by a class of flip-flops called the master-slave flip-flops.

→ The master-slave flip-flop was developed to make the synchronous operation more predictable, i.e., to avoid the problems of logic race in clocked flip-flops.

→ This improvement is achieved by introducing a known time delay (equal to the width of one clock pulse) between the time that the flip-flop responds to a clock pulse and the time the response appears at its output.

→ A master-slave flip-flop is also called a pulse-triggered flip-flop because the length of the time required for its output to change state equals the width of one clock pulse.

→ The master-slave or pulse-triggered flip-flop actually contains two flip-flops - a master flip-flop and a slave flip-flop.

→ The control inputs are applied to the master flip-flop and maintained constant for the set-up time t_s prior to the application of the clock pulse.

→ On the rising edge of the clock pulse, the levels on the control inputs are used to determine the output of the master.

→ On the falling edge of the clock pulse, the ~~levels on the control inputs~~ state of the master is transferred to the slave, whose outputs are Q and Q'.

→ Thus, the actual outputs of the flip-flop Q and Q' change just after the negative-going transition of the clock. So the master-slave flip-flops function very much like negative edge-triggered flip-flops.