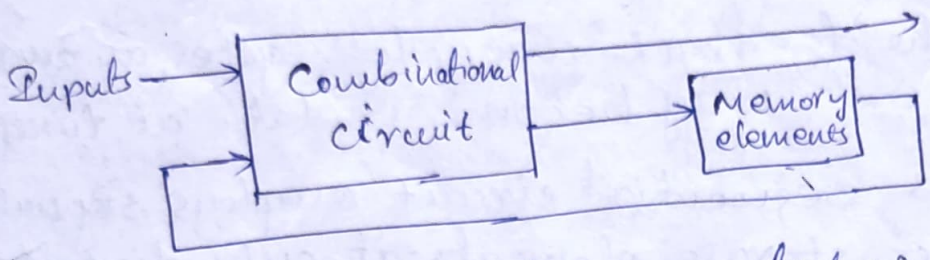
Sequential Circuits



Block diagram of Sequential Circuit

→ A block diagram of a sequential circuit consists of a combinational circuit to which storage elements are connected to form a feedback path.

→ The storage elements are devices capable of storing binary information.

→ The binary information stored in these (memory) elements at any given time defines the state of the sequential circuit at that time.

→ The sequential circuit receives binary information from external inputs, that together with the present state of the storage elements, determine the binary value of the outputs.

→ These external inputs also determine the condition for changing the state in the storage elements.

→ So, a sequential circuit is specified by a time sequence of inputs, outputs, and internal states. But the outputs of combinational logic depend only on the present values of the inputs.

→ There are two main types of sequential circuits, and their classification is a function of the timing of their signals: (1) synchronous sequential circuit (2) asynchronous sequential circuit.

→ A synchronous sequential circuit is a system whose behavior can be defined from the knowledge of its signals at discrete instants of time.

→ The behavior of an asynchronous sequential circuit depends upon the input signals at any instant of time and the order in which the inputs change.

→ The storage elements commonly used in asynchronous sequential circuits are time-delay devices.

→ In gate-type asynchronous systems, the storage elements consist of logic gates whose propogation delay provides the required storage. Thus, an asynchronous sequential circuit may be regarded as a combinational circuit with feedback.

→ Because of the feedback among logic gates, an asynchronous sequential circuit may become unstable at times.

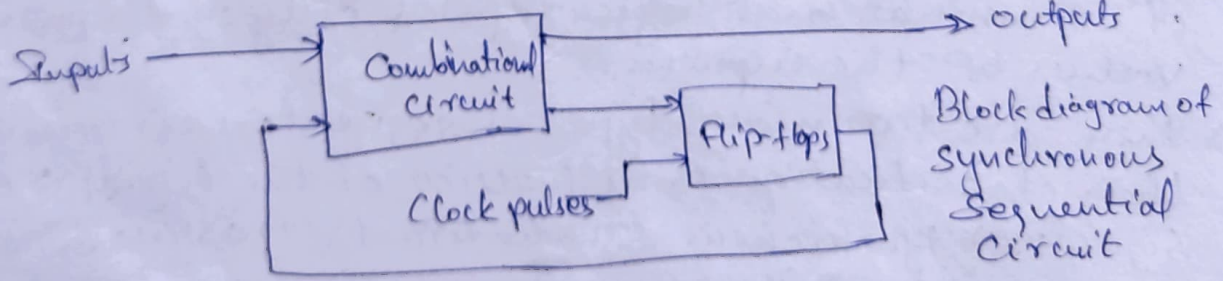
→ A synchronous sequential circuit employs signals that effect the storage elements at only discrete instants of time.

→ Synchronization is achieved by a timing device called clock generator, which provides a clock signal having the form of a periodic train of clock pulses.

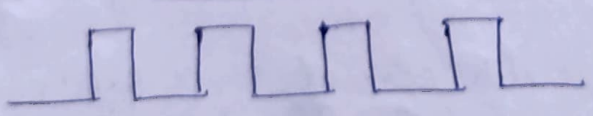
→ The clock pulses are commonly denoted by the identifiers clock and clk

→ The clock pulses are distributed throughout the system in such a way that storage elements are affected only with the arrival of each pulse.

→ Synchronous sequential circuits that use clock pulses to control storage elements are called clocked sequential circuits. They are called synchronous circuits because the activity within the circuit and the resulting updating of stored values is synchronized to the occurence of clock pulses.



Block diagram of synchronous sequential circuit



Timing diagram of clock pulses

→ The storage elements (memory) used in clocked sequential circuits are called flip-flops.

→ A flip-flop is a binary storage device capable of storing one bit of information.

→ In a stable state, the output of a flip-flop is either 0 or 1.

→ A sequential circuit may use many flip-flops to store as many bits as necessary.
→ The outputs are formed by a combinational logic function of the inputs to the circuit or the values stored in the flip-flops (or both).
→ The value that is stored in a flip-flop when the clock pulse occurs is also determined by the inputs to the circuit or the values presently stored in the flip-flop (or both).
→ The new value is stored (i.e., the flip-flop is updated) when a pulse of the clock signal occurs.
→ Before the occurence of clock pulse, the combinational logic forming the next value of the flip-flop must have reached a stable value.
→ If the clock (synchronizing) pulses arrive at a regular interval, the combinational logic must respond to a change in the state of the flip-flop in time to be updated before the next pulse arrives.
→ Propagation delays play an important role in determining the minimum interval between clock pulses that will allow the circuit to operate correctly.
→ A change in state of the flip-flops is initiated only by a clock pulse transition.
→ When a clock pulse is not active, the feedback loop between the value stored in the flip-flop and the value formed at the input to the flip-flop is effectively broken because the flip-flop outputs cannot change even if the outputs of the combinational circuit driving their inputs change in value.
→ Thus, the transition from one state to the next occurs only at predetermined intervals dictated by the clock pulses.