* Design of Asynchronous Counters:

Design steps:

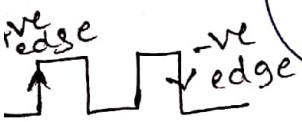
Step 1: Based on the description of the problem, determine the required no. of FFs. and desired Counting sequence

Step 2: Draw state diagram

Step 3: Select the type of FFs to be used and write the truth table (with clear signal (Reset signal) optional to be

NOTE: Asynchronous counters are designed by only two FFs Viz; J-K & T FFs.

~~Step 4:~~



Condition to get Toggling action
↳ $J = K = 1$; $T = 1$

NOTE: In order to design up counter
→ Q should be connected with the -ve edge of clk
→ $\bar{Q}$ should be connected with the +ve edge of clk

Step 5: Draw circuit diagram

Step 6: Draw Timing diagram

optional
Step 4: obtain minimal expression for R using K-ma

NOTE: In order to design down counter
→ Q should be connected with +ve edge of clock.
→ $\bar{Q}$ should be connected with -ve edge of clock.

* Design of a mod-8 asynchronous counter using JK FFs:

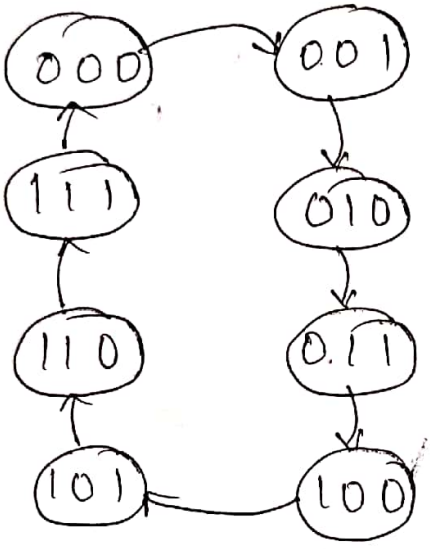
$2^n \geq N$ (n → no. of bits, N → count No.)

Step 1: No. of FFs = 3 ; Up count.

No. of states = 8 (000, 001, 010, 011, 100, 101, 110, 111)

All are valid states

Step 2: State diagram



Step 3: JK FFs are selected. J = K = 1 for all FFs

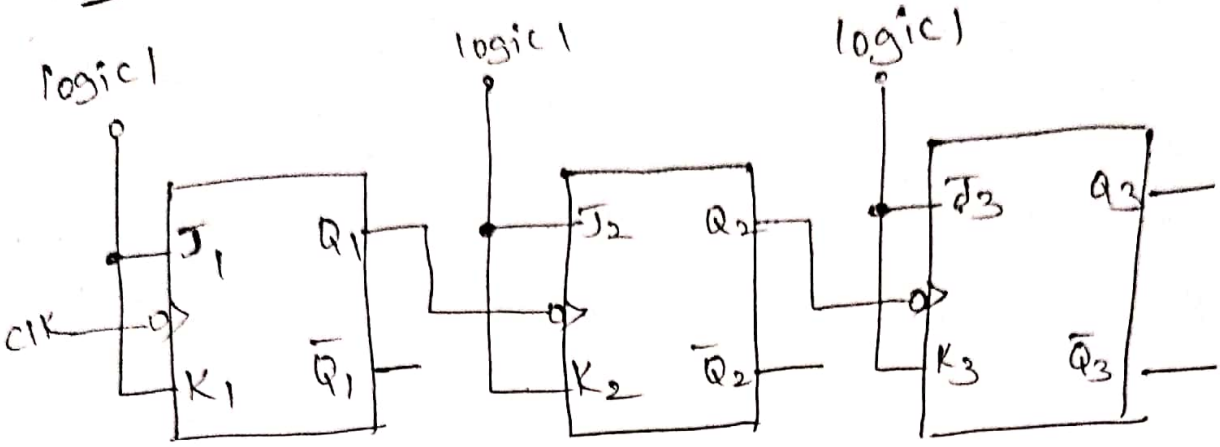
CLK Pulses	State Q_3	Q_2	Q_1	Decimal equivalent	Reset
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	2	0
3	0	1	1	3	0
4	1	0	0	4	0
5	1	0	1	5	0
6	1	1	0	6	0
7	1	1	1	7	1
8	0	0	0	0	

Step 4: K-map for R

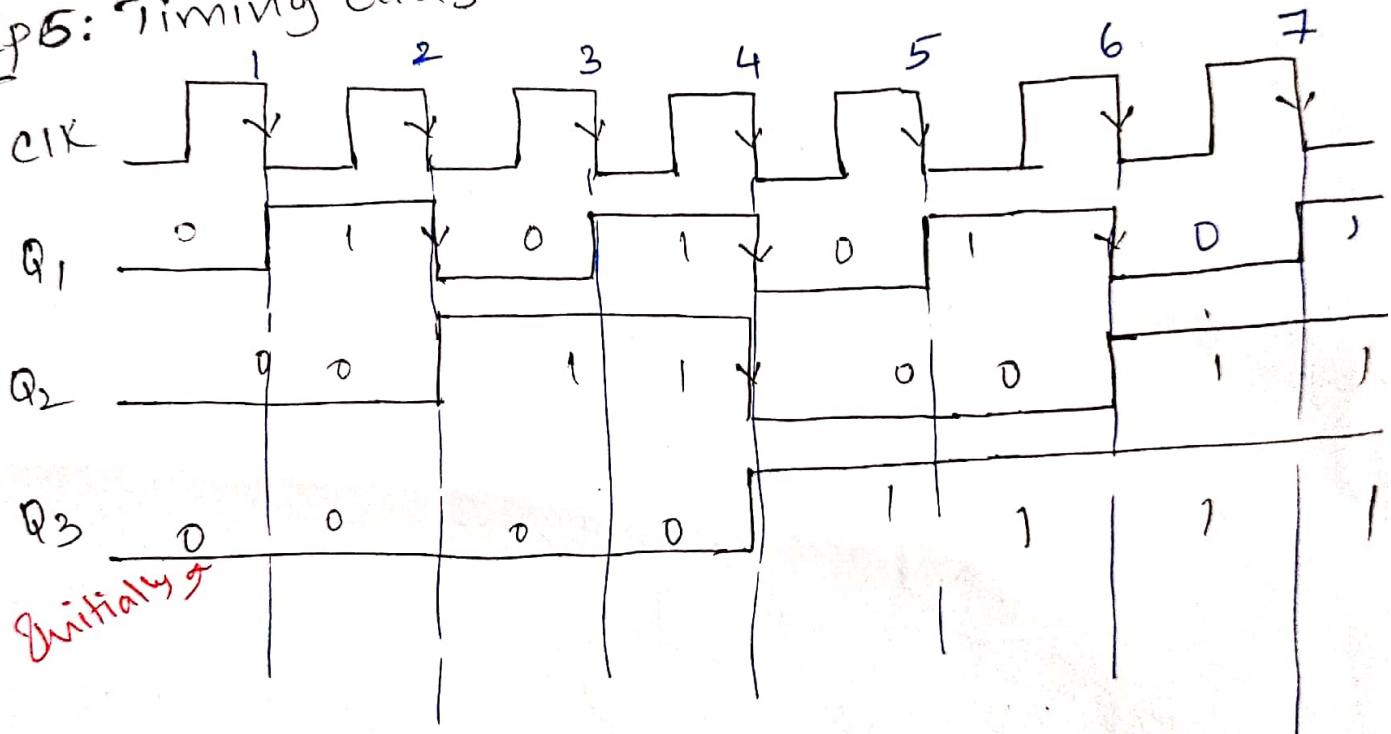
Q_3 \ Q_2Q_1	00	01	11	10
0				
1			1	

$R = Q_3 Q_1$

Step 5: logic diagram



Step 6: Timing diagram



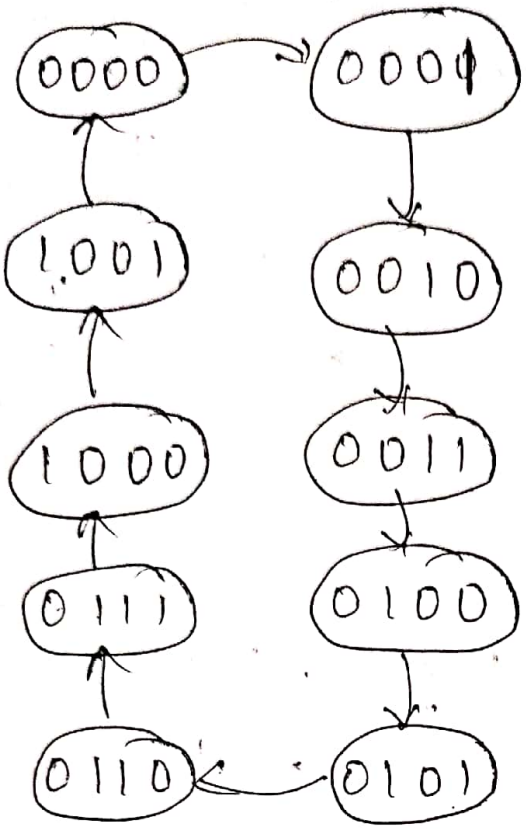
* Design of a Mod-10 Asynchronous Counter using JK FFs:

Step 1: No. of FFs = 4

No. of states $= 2^4 = 16$ ie; from 0000 to 1111

Valid states will be from 0000 to 1001.

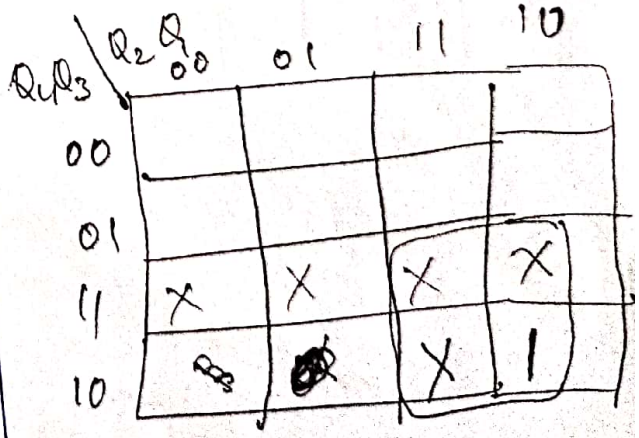
Step2: State diagram



Step3: JK FFs are selected ; $J = K = 1$ for all FFs

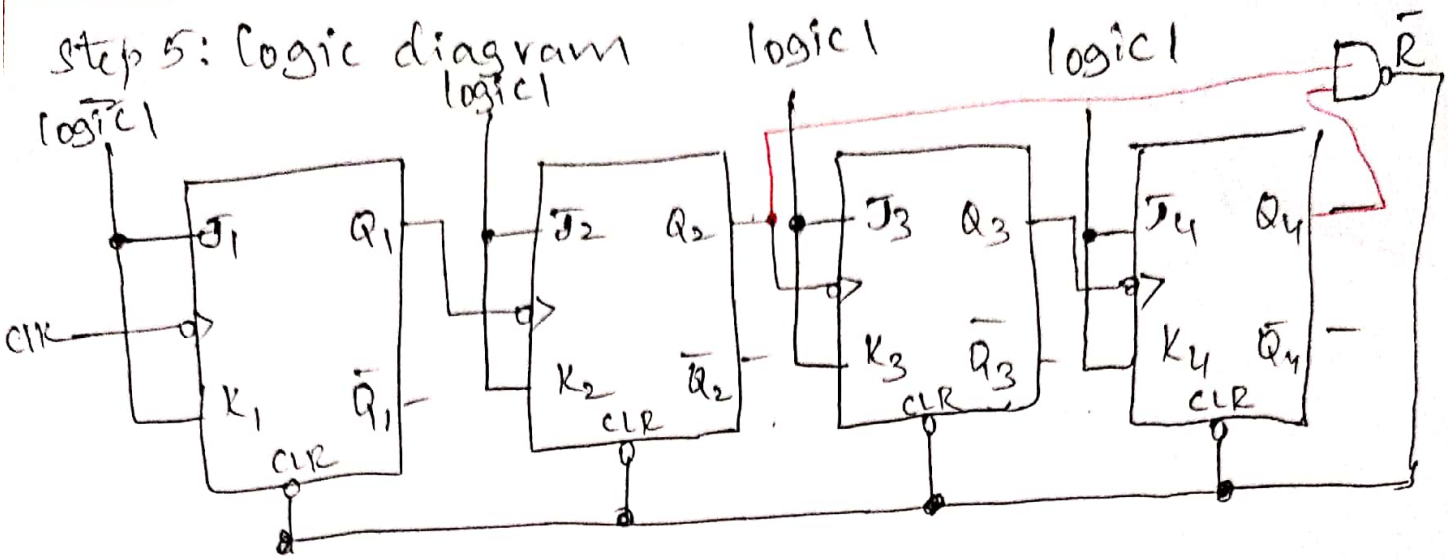
CLK Pulses	State $Q_4\ Q_3\ Q_2\ Q_1$	Reset/clear R
0	0 0 0 0	0
1	0 0 0 1	0
2	0 0 1 0	0
3	0 0 1 1	0
4	0 1 0 0	0
5	0 1 0 1	0
6	0 1 1 0	0
7	0 1 1 1	0
8	1 0 0 0	0
9	1 0 0 1	0
10	0 0 0 0	1
	0 0 0 1	

Step4 : K Map for R

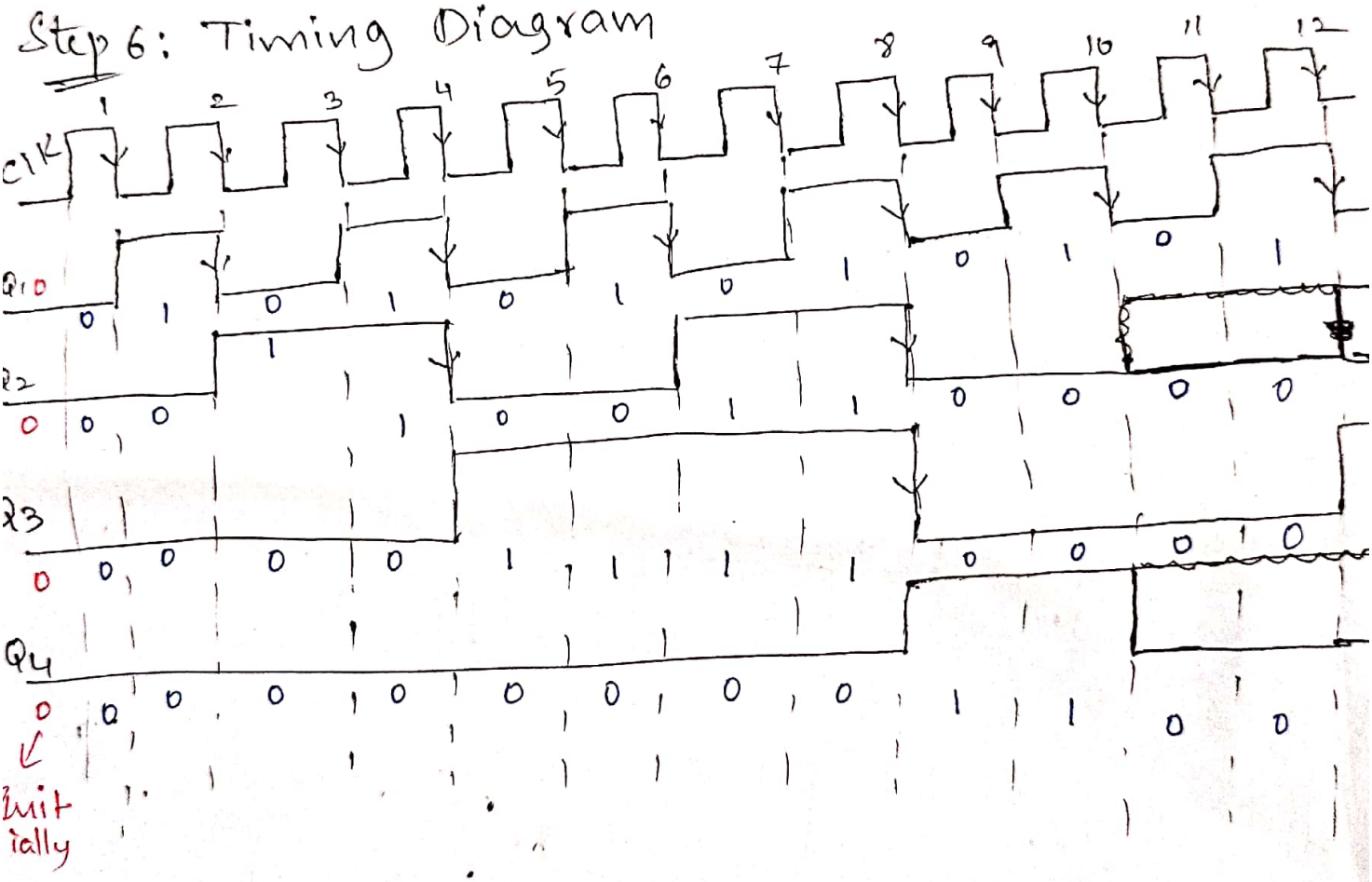


$R = Q_4 Q_2$

Step 5: Logic diagram



Step 6: Timing Diagram



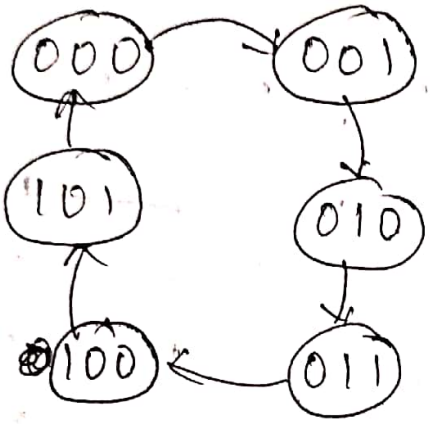
* Design of a mod-6 asynchronous counter using T FFs:

Step 1: No. of FF = 3 ; Up count

No. of states = 2^3 = 8 (000, 001, 010, 011, 100, 101, 110, 111)

110 & 111 are invalid states.

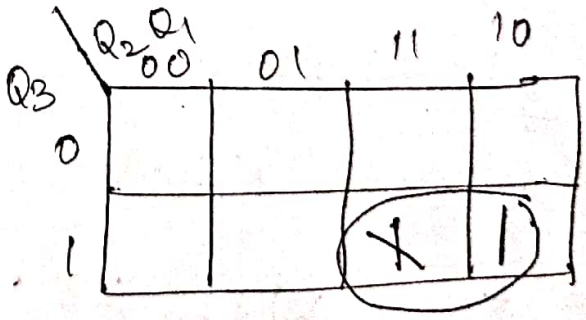
Step 2: State diagram



Step 3: T FFs are selected. T = 1 for all FFs

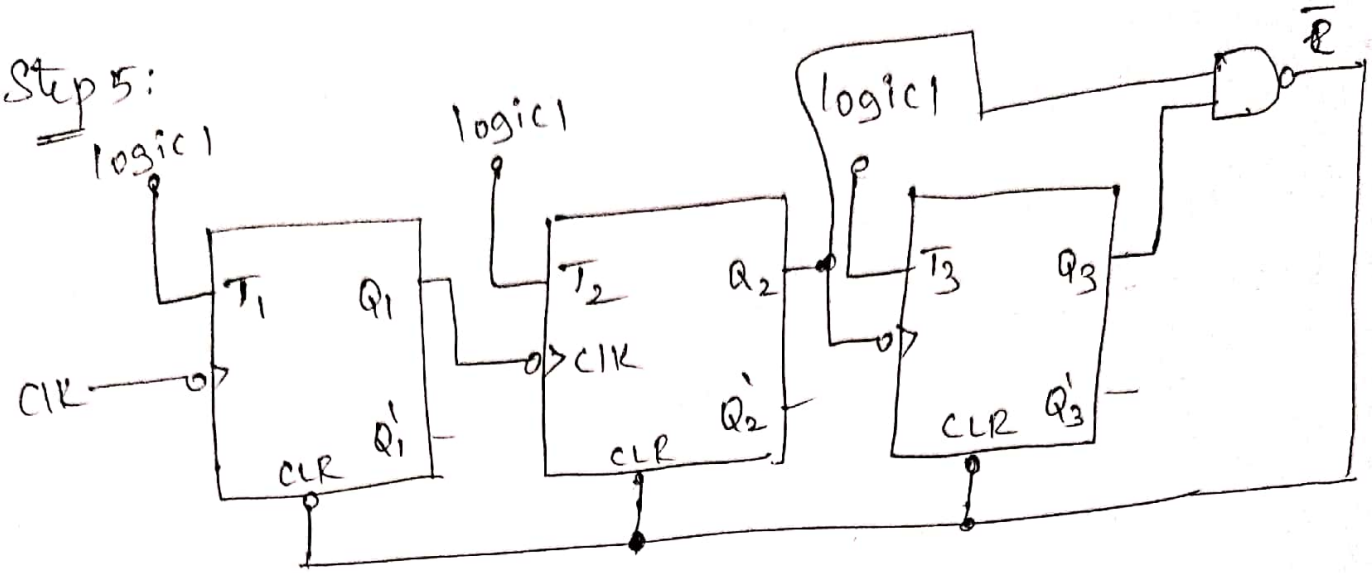
CLK Pulses	state Q_3 Q_2 Q_1	Reset/CLR R
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	0
5	1 0 1	0
	↓ ↓ ↓	
	0 0 0	1
6	0 0 1	

Step 4: K Map for R

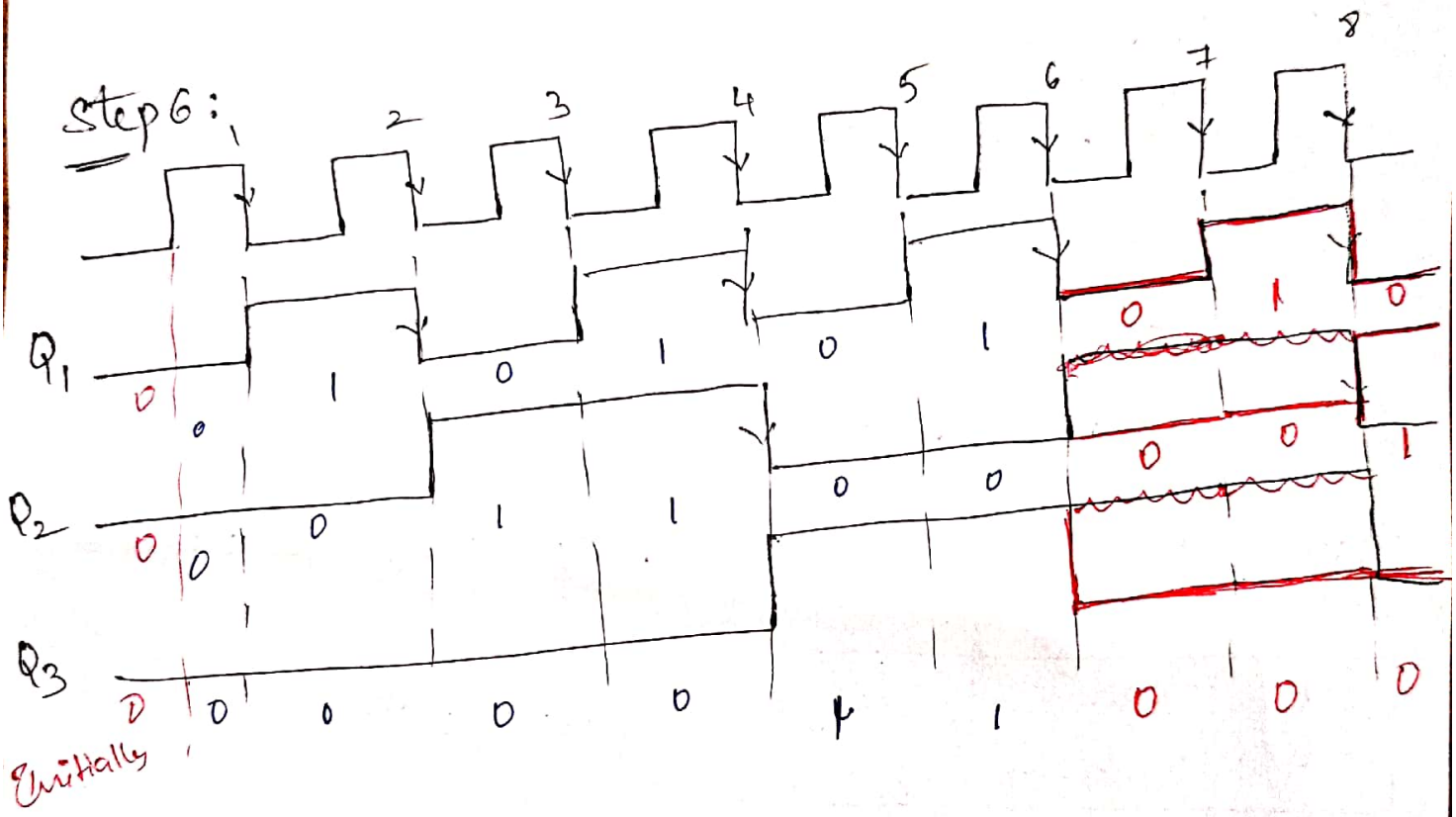


$R = Q_3 Q_2$

Step 5:



Step 6:



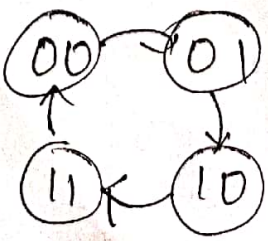
Eventually

* Two-bit Ripple up-counter using Negative edge-triggered FFs:

Step 1: No. of FFs = 2 ; Up count

No. of states $= 2^2 = 4$ (00, 01, 10, 11)

Step 2: State diagram



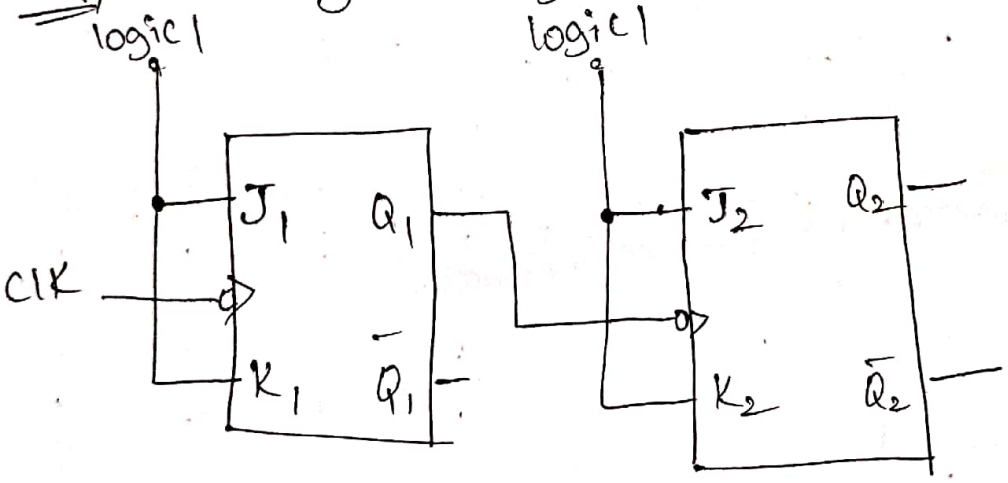
Step3: JK FFs are selected.

CLK Pulses	State Q_2	Q_1
0	0	0
1	0	1
2	1	0
3	1	1

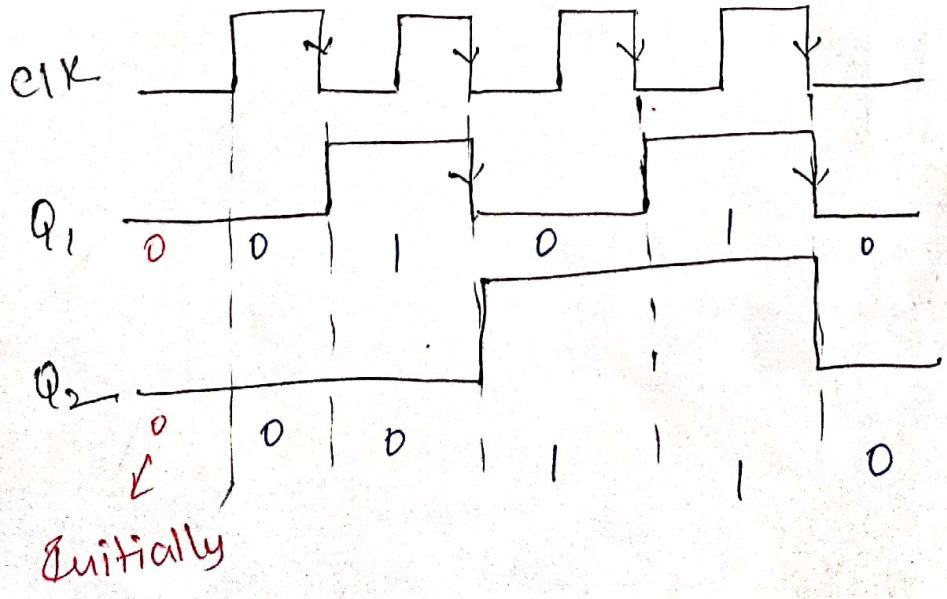
$J = K = 1$ for all FFs.

Step4: Not needed

Step5: Logic diagram



Step6: Timing Diagram

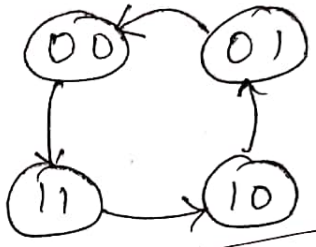


* Two-bit Ripple Down-Counter Using Negative edge-triggered flip flops:

Step 1: No. of FFs = 2 ; Down Count

No. of states = $2^2 = 4$ (00, 01, 10, 11)

Step 2: State diagram



Step 3: JK FFs are selected.

CLK Pulses	State Q_n	State $\bar{Q}_n$

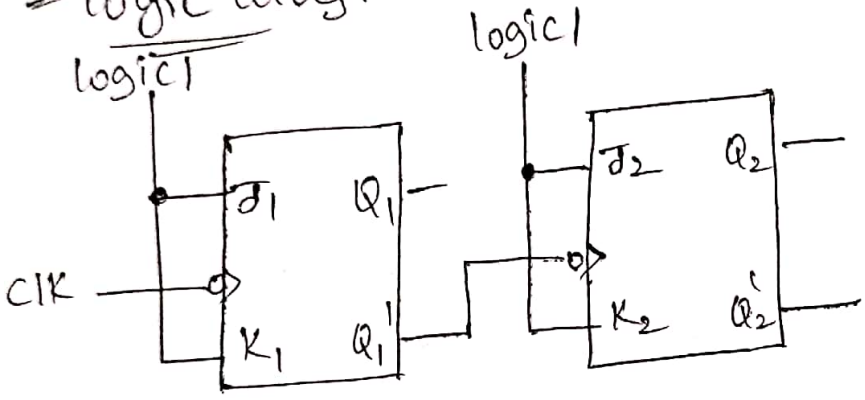
Step 4: K Map not needed

CLK Pulses	Q_2	Q_1	$\bar{Q}_2$	$\bar{Q}_1$
0	1	1	0	0
1	1	0	0	1
2	0	1	1	0
3	0	0	1	1

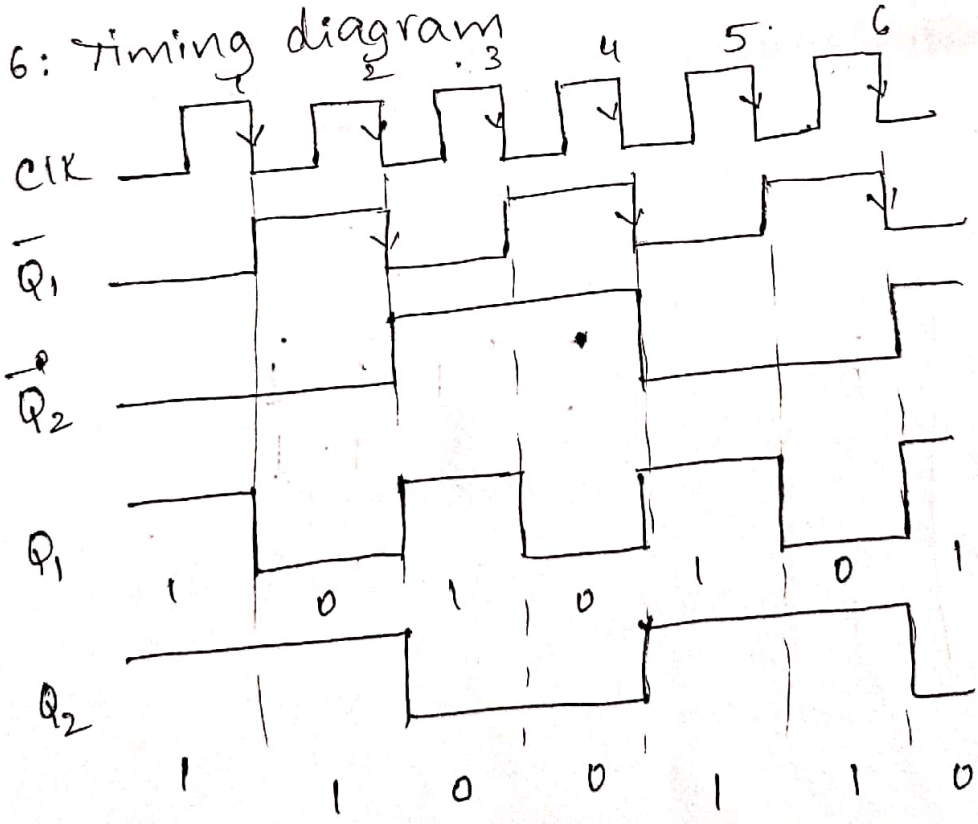
o/ps to be read at Q_2 & Q_1.

Steps:

Step 5: logic diagram



Step 6: Timing diagram



* Two-bit ripple Up-down Counter:

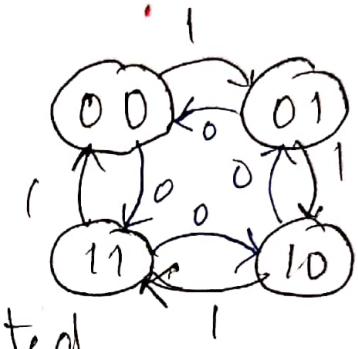
Step 1: No. of FFs = 2 ; Up & Down count

let's say, if M=1, circuit works as Up Counter

M=0, circuit works as Down Counter

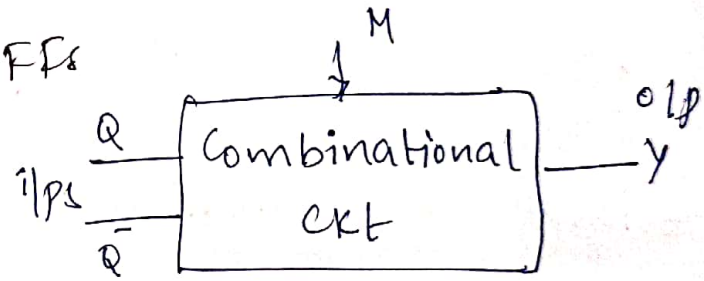
Where M → Mode signal/Control signal

Step 2: State diagram



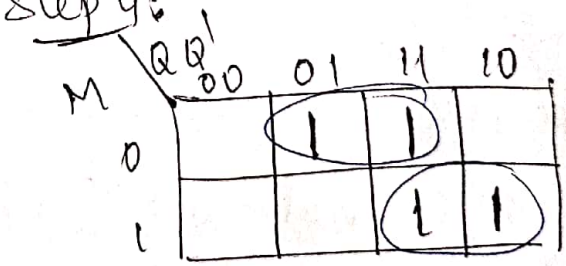
Step 3: JK FFs are selected

J = K = 1 for all FFs



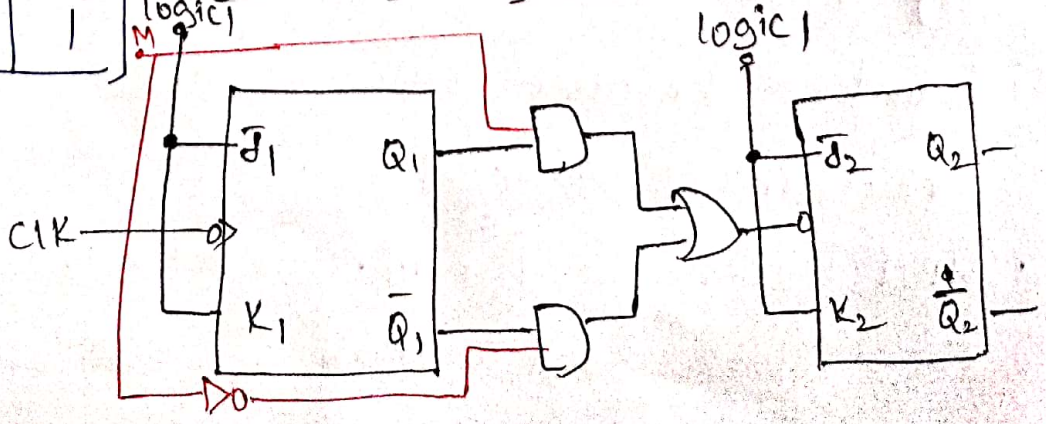
M	Q	Q̄	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Step 4:

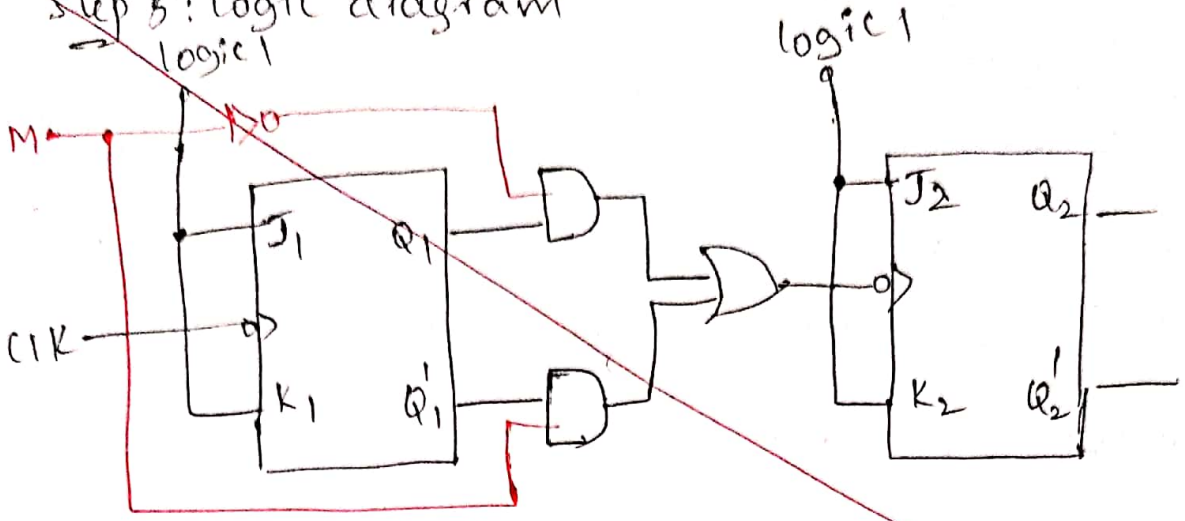


$$Y = MQ + M'Q'$$

Step 5 : logic diagram



Step 5: Logic diagram



* Shift Register Counters:

↳ Design and operation of Ring Counter

↳ Design and operation of Twisted-Ring Counter

- One of the applications of shift registers is that they can be arranged to form several types of counters.
- Shift register counters are obtained from serial-in, serial-out shift registers by providing feedback from the o/p of the last FF to the i/p of the first FF These devices are called Counters because they exhibit a specified sequence of states.
- Most widely used shift register counters are ring counter and twisted ring counter.