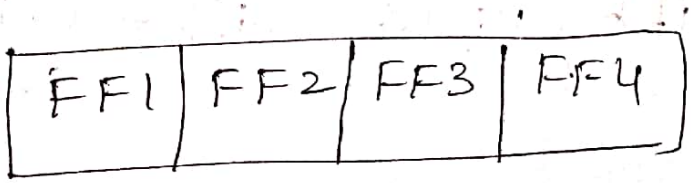
UNIT - IV

Registers and Counters

* Introduction:

- Flip-flop is a 1-bit memory cell.
- TO increase the storage capacity, a group of flip flops are needed. This group of flip flops is known as REGISTER
- The n-bit register consists of "n" no. of FFs and is capable of storing n-bits.
- A Flip-flop is referred to as single-bit register

EX: 4-bit register → requires 4 FF



- A register is a digital circuit with two basic fns: Data storage and Data Movement
- A shift register provides the data movement function
- A shift register "shifts" its o/p once every clock cycle

Definition of a Shift Register:

- A shift register is a group of flipflops set up in a linear function with their i/p and o/ps are connected together in such a way that the data shifted from one device to another when the circuit is active

Shift Register Types:

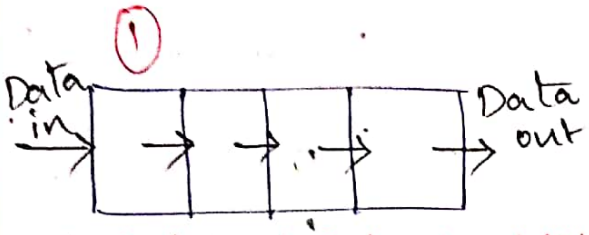
1. Serial in Serial out (SISO)
2. Serial in parallel out (SIPO)
3. Parallel in parallel out (PIPO)
4. Parallel in serial out (PISO)

Shift Register Types w.r.t direction:

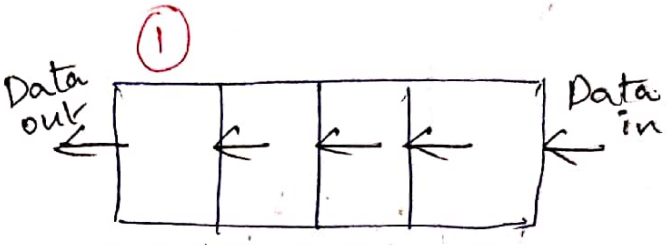
1. Left shift / Right shift → Unidirectional shift register
2. Bidirectional shift register → shifts both left & right
3. Universal shift register
   ↳ shifts both left & right and also have parallel loading capabilities

Data Movement:

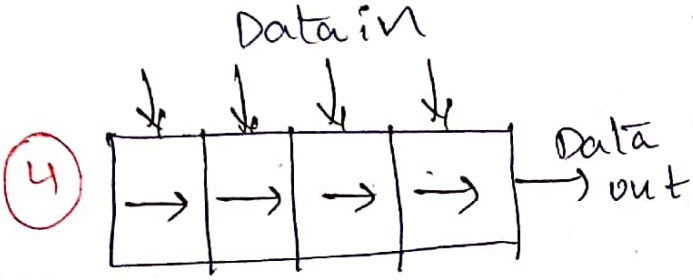
- The bits in a shift register can move in any of the following manners:



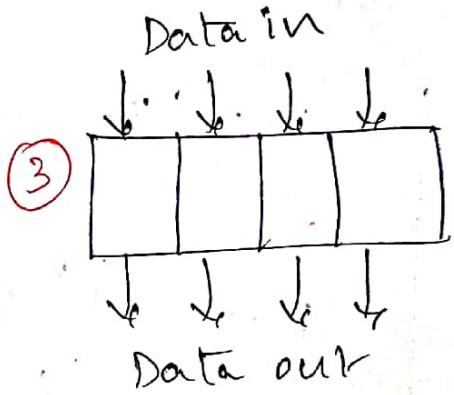
Serial in serial out, shift right shift register



Serial in serial out, Shift left shift register



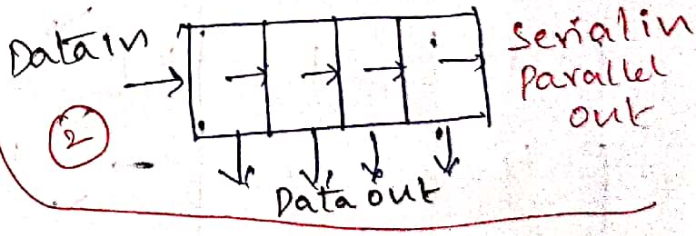
Parallel in Serial out, Shift right Shift register



Parallel in parallel out Shift register

(1) SISO:

- Serial in serial out



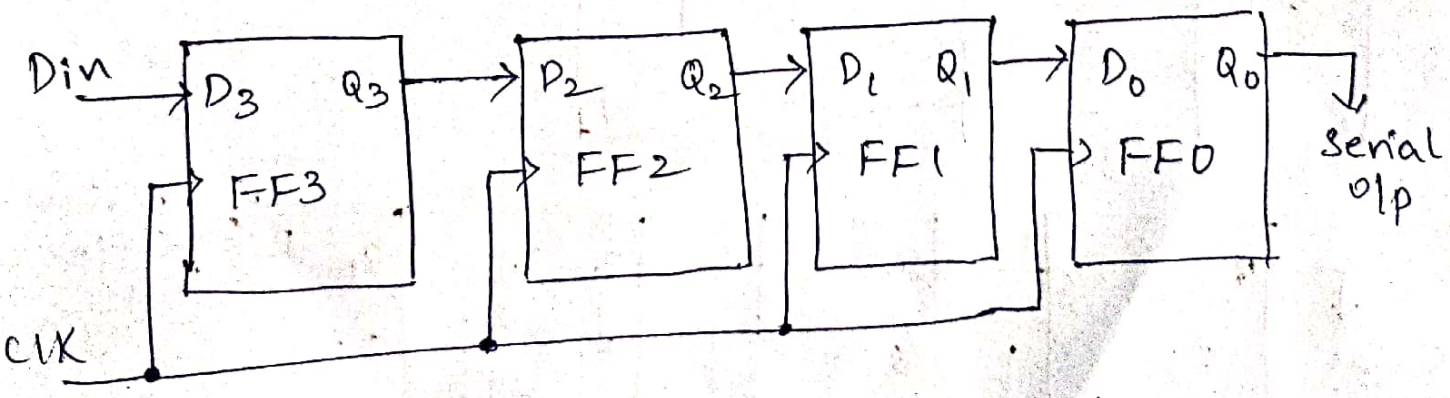


Fig: SISO, shift right Register 4-bit

CLK	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
↑	1	0	0	0
↑	1	1	0	0
↑	0	1	1	0
↑	1	0	1	1
↑	–	1	0	1
↑	–	–	1	0
↑	(~~0~~)	–	–	1

1011
MSB LSB

DFF TT

CLK	D	Q_{n+1}
0	X	Q_n
↑	0	0
↑	1	1

(or)

CLK	Input	Q_3	Q_2	Q_1	Q_0
0	–	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	0	0	1	1	0
4	1	1	0	1	1
5	–	–	1	0	1
6	–	–	–	1	0
7	–	–	–	–	1

(2N-1) clock pulses are required for SISO.

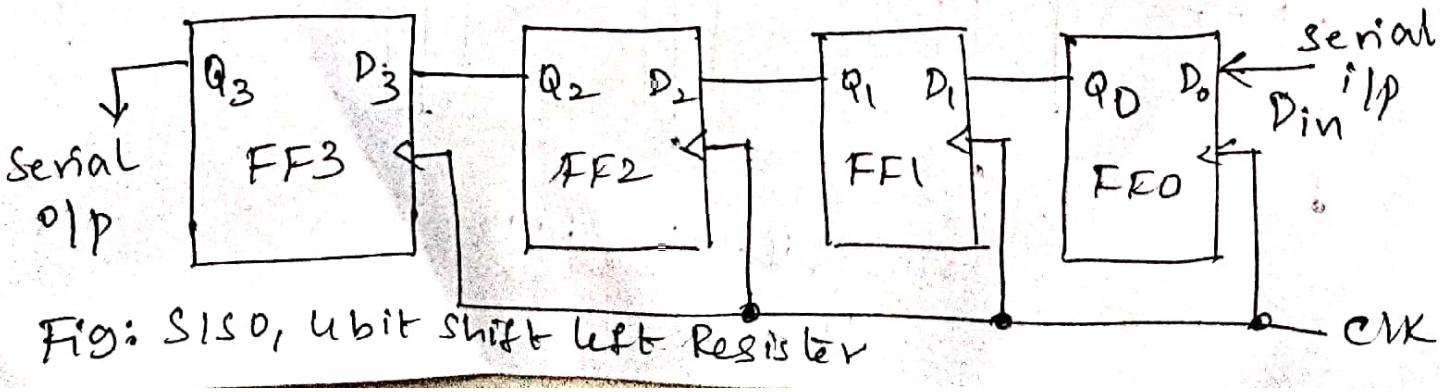


Fig: SISO, 4bit shift left Register

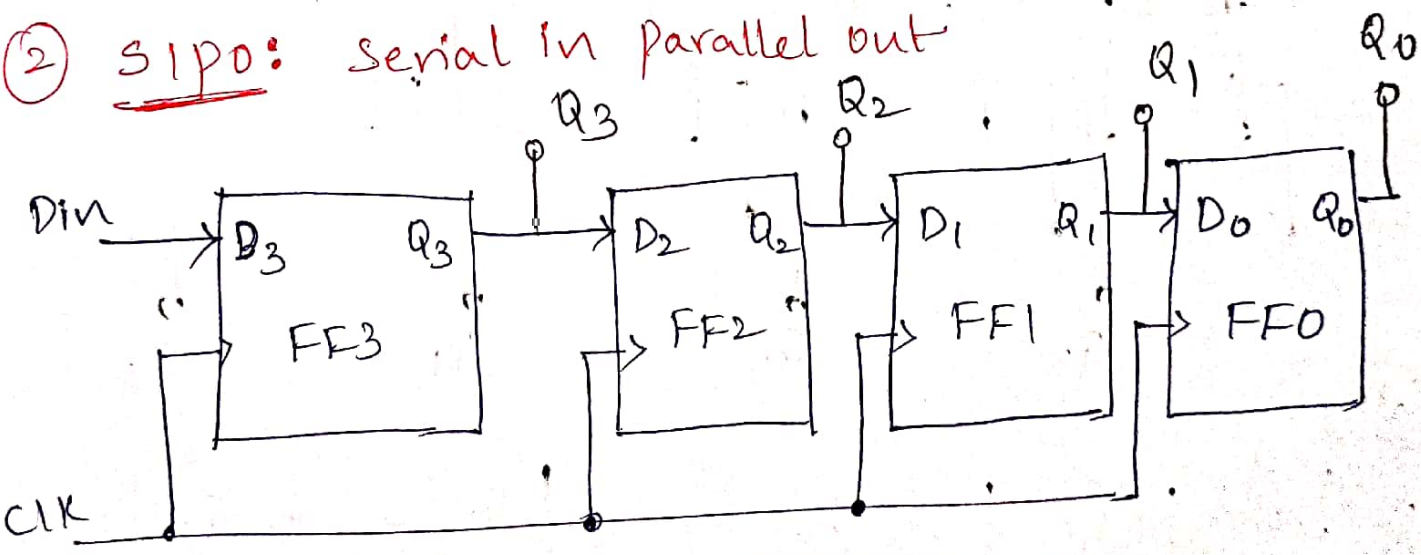
(or)

③ Data 2, 1 0 1 1 (MSB ... LSB)

CLK	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	1	1	0	0	1	1	0	0
3	0	1	1	0	0	1	1	0
4	1	0	1	1	1	0	1	1
5	0	1	0	1	0	1	0	1
6	0	0	1	0	0	0	1	0
7	0	0	0	1	0	0	0	1

1 0 1 1 (MSB ... LSB)

② SIPO: Serial in parallel out



CLK	input	Q_3	Q_2	Q_1	Q_0
Initially → 0	0	0	0	0	0
1	1	1	0	0	0
2	1	1	1	0	0
3	0	0	1	1	0
4	1	1	0	1	1

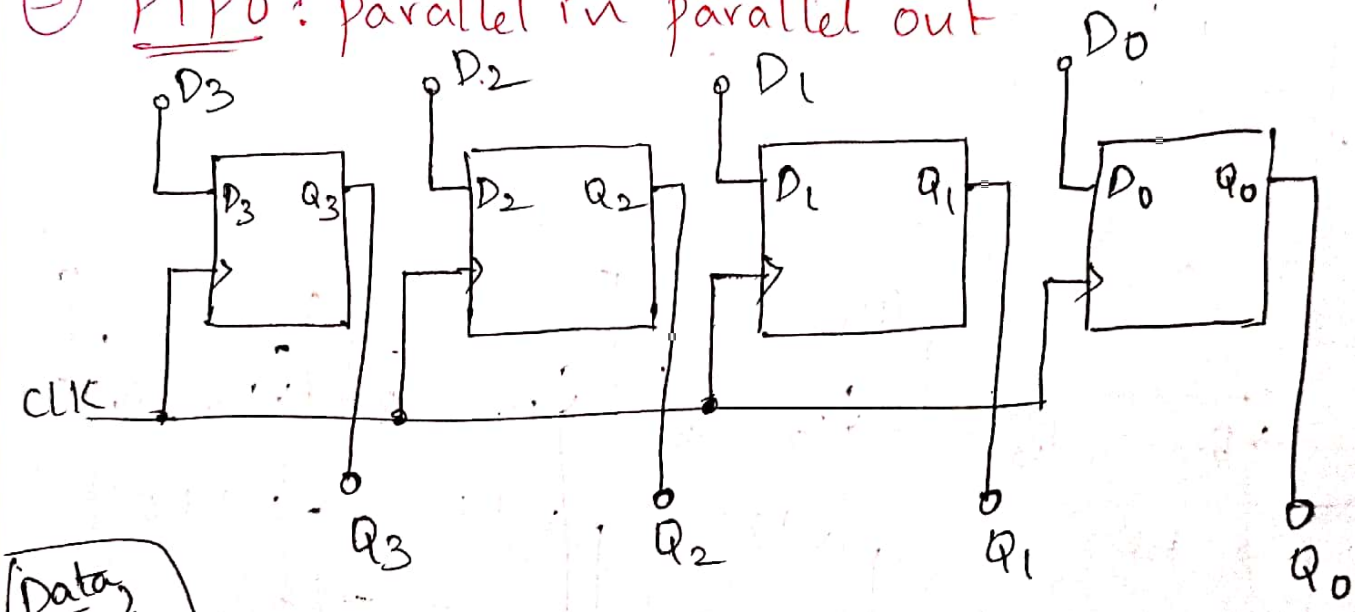
1 0 1 1 (MSB ... LSB)

For n bit transmission n clock pulses are required in SIPO

Data
1 0 1 1
MSB LSB

CLK	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0
2	1	1	0	0	1	1	0	0
3	0	1	1	0	0	1	1	0
4	1	0	1	1	1	0	1	1

③ PIPO : parallel in parallel out

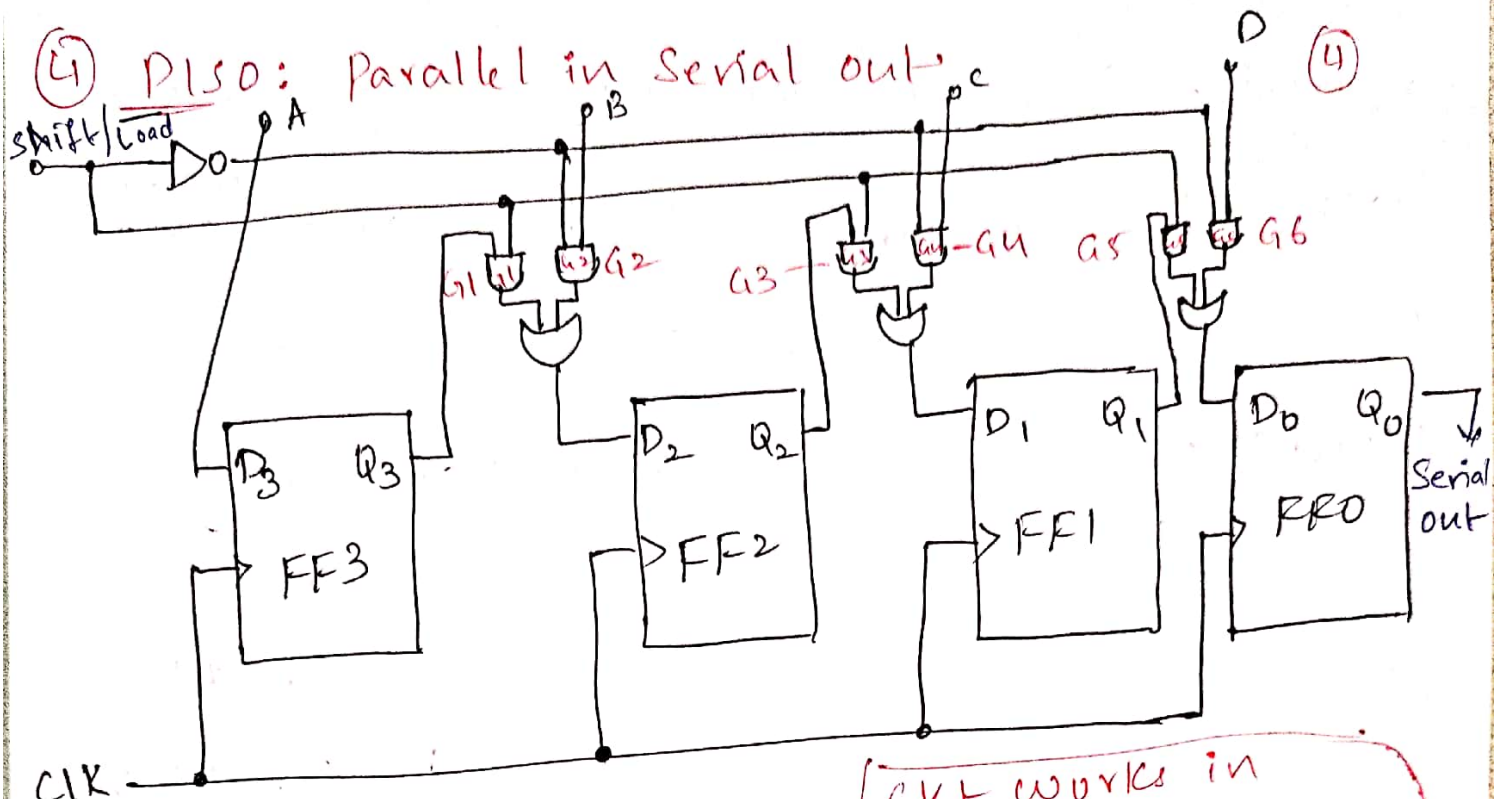


Data
1 0 1 1
MSB LSB

CLK	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0
1	1	0	1	1	1	0	1	1

In PIPO,
1 clock pulse is required for data transmission

(4) PISO: Parallel in Serial out (4)



CKT works in
- load mode and
- shift mode

- The Shift/load allows
  - the data to be entered in parallel form into the register and
  - the data to be shifted out serially from terminal Q_0

Case(i): If Shift/load = 1

- If Shift/load = 1, CKT works in ~~load~~ shift mode
  AND gates G_2, G_4, G_6 will be disabled and
  AND gates G_1, G_3, G_4 will be operational.
- Now the i/ps of the FFs becomes : A for FF3
  Q_3 for FF2
  Q_2 for FF1
  Q_1 for FF0

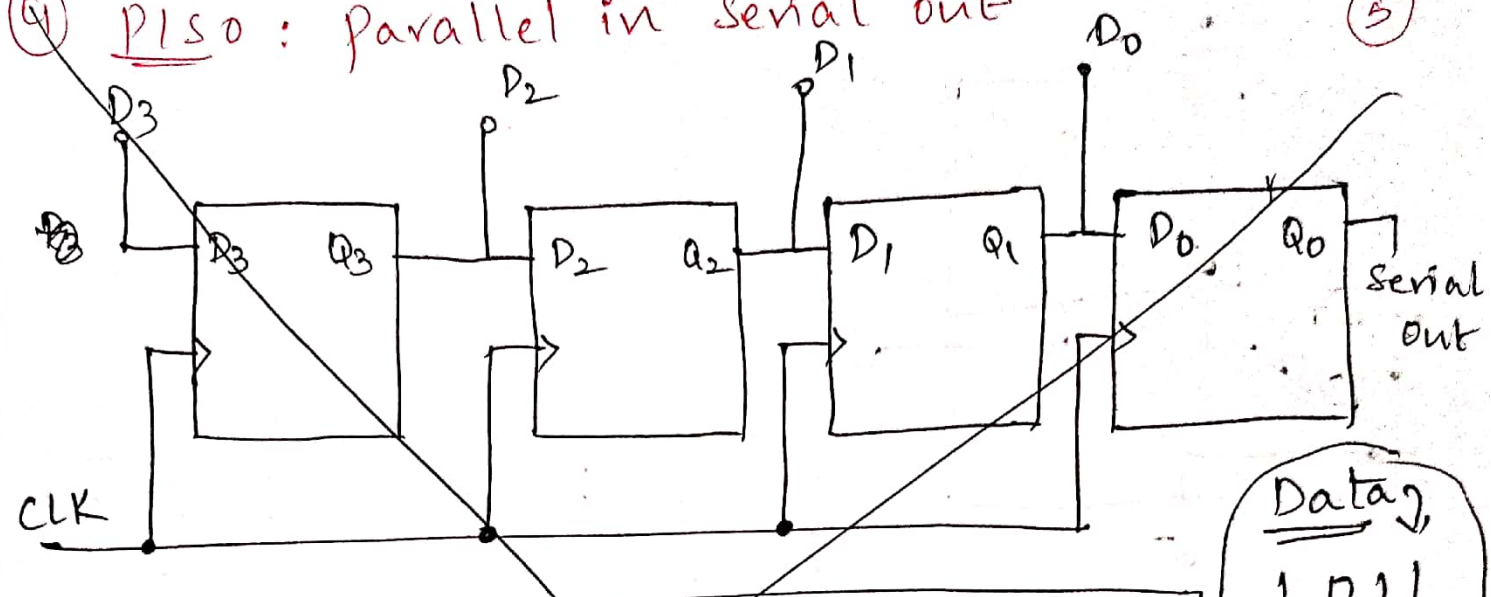
Case (ii): If Shift/$\overline{load}$ = 0

- If Shift/$\overline{load}$ = 0, ckt works in load mode whereas AND gates G_2, G_4, G_6 will be enabled AND gates G_1, G_3, G_5 will be disabled.

Now the i/ps of FFs becomes: A for FF3
B for FF2
C for FF1
D for FF0

- In parallel-in, serial-out shift register, the data bits are entered simultaneously into their respective stages on parallel lines, rather than on a bit-by-bit basis on one line as with serial data i/ps, but the data bits are transferred out of the register serially i.e, on a bit-by-bit basis over a single line

PISO : Parallel in Serial out

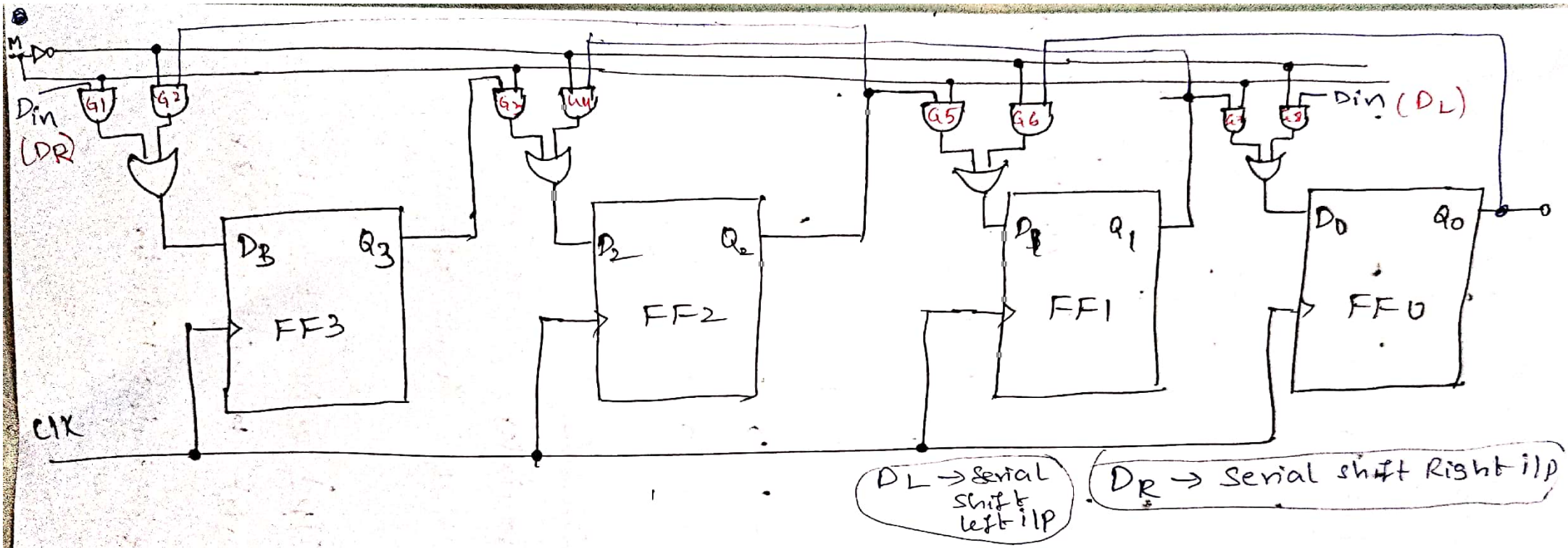


Data,
1 0 1 1
MSB LSB

CLK	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0
1	1	0	1	1	1	0	1	1
2	0	1	0	1	0	1	0	1
3	0	0	1	0	0	0	1	0
4	0	0	0	1	0	0	0	1

* Bidirectional Shift Registers:

- A bidirectional shift register is one in which the data bits can be shifted from left to right or from right to left
- If (M → Mode Control i/p) logic ckt works as a
  - M=1 → shift-right shift register
  - M=0 → shift-left shift register



- The bidirectional operation is achieved by using mode signal and two AND gates and one OR gate for each stage.

Case(i) : M=1

→ If M=1, AND gates G_2, G_4, G_6, G_8 will be ~~get~~ disabled where as AND gates G_1, G_3, G_5, G_7 will be enabled.

→ Now, the i/ps of the FFs ~~from right~~ will be : ~~I/p~~ D_R for FF3

- Q_3 for FF2
- Q_2 for FF1
- Q_1 for FF0

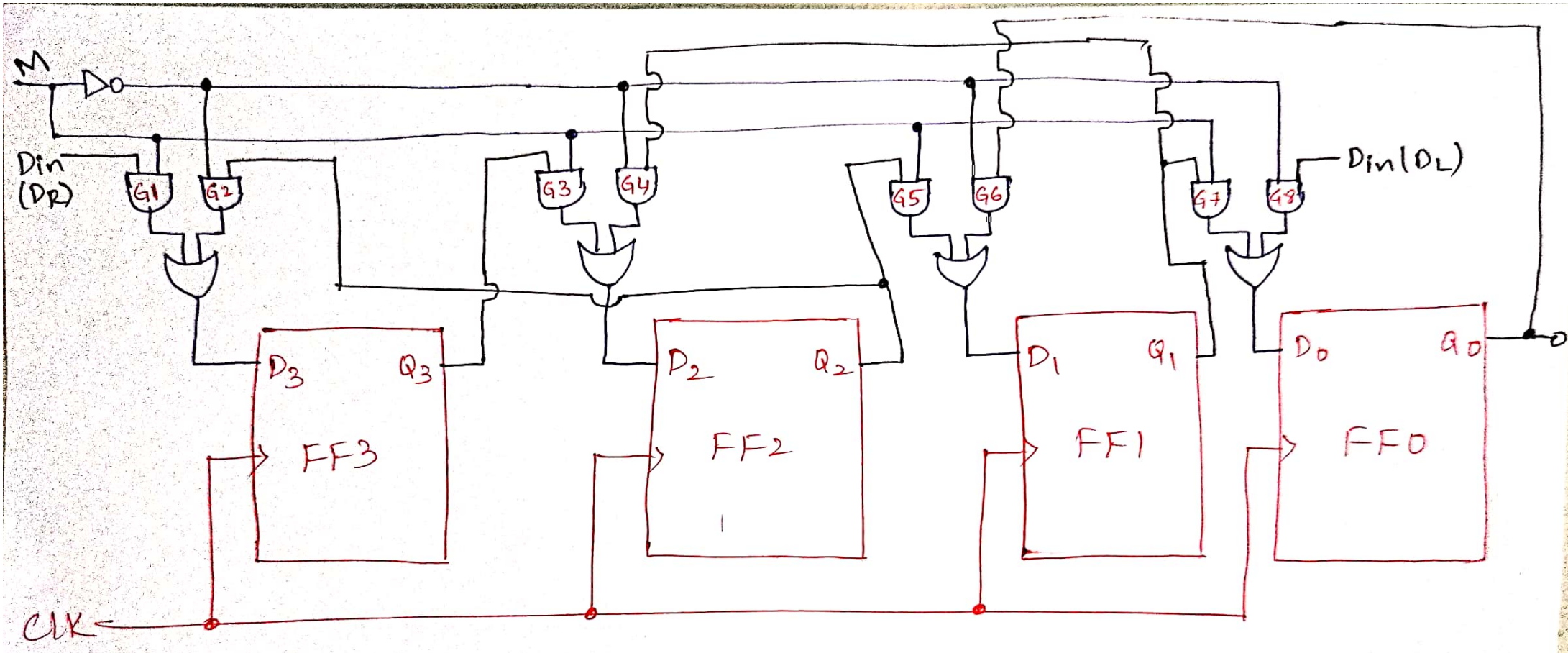


Fig: Logic diagram of a 4-bit bidirectional shift register

$D_L \rightarrow$ Serial shift left i/p

$D_R \rightarrow$ Serial shift right i/p

} $\rightarrow$ Din

- The data is first stored in FF3, then FF2, FF1, and FF0. Ie; data is getting shifted from right to left ie; shift-right operation

Case(ii): M=0

- Now AND Gates G_2, G_4, G_6, G_8 are operational where as AND gates G_1, G_3, G_5, G_7 will be disabled
- The i/ps of the FFs will be: D_L for FF0
  Q_0 for FF1
  Q_1 for FF2
  Q_2 for FF3
- Here, the data is first stored in FF0, then FF1, FF2 and FF3. Ie; data is shifting to left side so. shift-left operation.