UNIT - 5

LOGIC FAMILIES and A/D and D/A Converters

Introduction:

- There are two types of semiconductor transistor devices:
  - Bipolar
  - unipolar
- Various digital functions are being fabricated in a variety of forms using Bipolar and unipolar technologies.
- A group of compatible ICs with the same logic levels and supply voltages for performing various logic functions have been fabricated using a specific circuit configuration which is referred to as a logic family.

Classification of Integrated Circuits:

- Digital ICs are classified ~~either~~ according to the complexity of the circuit, the relative number of individual basic gates it would require to build the circuit on the chip.
- The classification of digital ICs are given below

1) Small-scale Integration (SSI): It Describes fixed-function ICs that have 12 equivalent gates circuits (up to 99 no. of components) on a single chip, and they include basic gates and flip flops.

2) Medium-scale Integration (MSI):

It describes integrated circuits that have from 12 to 99 equivalent gates or a (100 to 999 no. of components) on a chip.

They include logic functions such as encoders, decoders, counters, registers, multiplexers, arithmetic circuits, small memories etc.

3) Large-scale Integration (LSI):

It is a classification of IC with complexities of 100 to 9,999 equivalent gates (1000 to 9,999 no. of components) per chip, including memories.

4) Very Large-scale Integration (VLSI):

It describes integrated circuits with complexities of 10,000 to 99,999 equivalent gates (above 10,000 no. of components) per chip.

5) Ultra large-scale Integration (ULSI):

It describes very large memories, larger micro processors, and larger single-chip computers.

The complexities of 100,000 equivalent gates and greater are classified as ULSI.

Integrated Circuit Technologies:

- The types of transistors with which all integrated circuits are implemented are either bipolar junction transistors & MOSFETS (Metal-oxide semiconductor field-effect transistors)
- Two types of digital Circuit Technologies are
  - Bipolar Logic families (or) Bipolar circuit Technology
  - Unipolar logic families (or) Unipolar Circuit Technology
- Bipolar logic families:
  - The main elements of a bipolar IC are Resistors, diodes and transistors.
  - Basically, there are two types of operation in Bipolar IC:
    1. saturated, and
    2. Non-saturated
  - In saturated logic, the transistors in the ICs are driven to saturation, whereas in the case of non-saturated logic, the transistors are not driven into saturation.
  - The saturated Bipolar logic families are:
    1. Resistor-Transistor Logic (RTL)
    2. Direct-coupled transistor Logic (DCTL)
    3. Integrated-Injection Logic (I^2L)
    4. Diode-transistor Logic (DTL)
    5. High-Threshold Logic (HTL), and

6. Transistor - Transistor Logic (TTL)

- The non-saturated bipolar logic families are;

1. Schottky TTL, and
2. Emitter-coupled logic (ECL)

* ~~Bipolar logic families~~:

- Among all the above Bipolar logic families TTL and ECL are important logic families.
- Of these two, TTL is more widely used.

• Unipolar Logic families:

MOS devices are unipolar devices and only MOSFETs are employed in MOS Logic circuits.

- The MOS logic families are:

1. PMOS
2. NMOS, and
3. CMOS

While in PMOS, only P-channel MOSFETs are used and in NMOS, only n-channel MOSFETs are used, in Complementary MOS (CMOS), both P- and n-channel MOSFETs are employed and are fabricated on the same Si chip.

Among all the above unipolar logic families NMOS and CMOS are important logic families

Microprocessors use MOS Technology.

- SSI and MSI circuits are available in both TTL and CMOS.
- LSI, VLSI, and ULSI are implemented with CMOS & NMOS because it requires less area on a chip and also consumes less power.
- CMOS and TTL are the dominant digital IC technologies in use for logic devices.

They differ only in the type of circuit components and values of parameters and not in the basic logic operations.

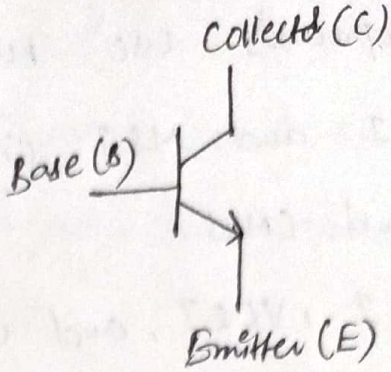
A CMOS AND gate has the same logic operation as a TTL AND gate.

The difference in CMOS and TTL is in performance characteristics such as switching speed (propagation delay), power dissipation, noise immunity, and other parameters.

→ TTL Circuits :

- The bipolar junction transistor (BJT) is the active switching element used in all TTL circuits.
- The symbol for an npn BJT with its three terminals base, emitter and collector is shown below

- A BJT has two junctions, base-emitter junction and the base-collector junction.



- The basic switching operation is as follows:

When the base is approximately 0.7V more positive than the emitter and when sufficient current is provided into the base, the transistor turns ON and goes into saturation.

In saturation, the transistor ideally acts like a closed switch between the collector and the emitter.

When the base is less than 0.7V more positive than the emitter, the transistor turns off and becomes an open switch between the collector and the emitter.

i.e a HIGH on the base turns the transistor on and makes it a closed switch.

A LOW on the base turns the transistor off and makes it an open switch.

In TTL, some BJTs have multiple emitters.

TTL Inverter:

- The logic function of an inverter or any

- The below figure shows a standard TTL circuit for an inverter.

- In this figure Q_1 is the input coupling transistor,

and D_1 is the input clamp diode.

. Transistor Q_2 is called a phase splitter, and the combination of Q_3 and Q_4 form the output circuit often referred to as a totem-pole arrangement.

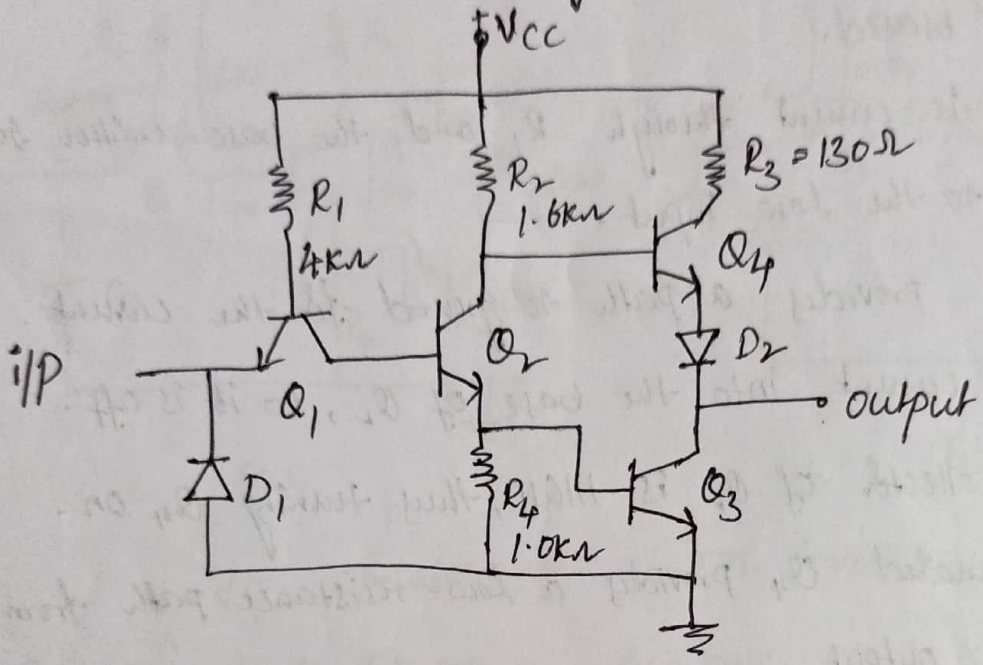


fig. standard TTL inverter circuit

. When the input is a HIGH, the base-emitter junction of Q_1 is reverse biased, and the base-collector junction is forward biased.

. This condition permits current through R_1 and the base collector junction of Q_1 into the base of Q_2, thus driving Q_2 into saturation.

. As a result, Q_3 is turned on by Q_2, and its collector voltage, which is the output, is near ground potential.

∴ Low output for a HIGH input.

- At the same time, the collector of Q_2 is at a sufficiently low voltage level to keep Q_4 off.
- When the input is Low, the base-emitter junction of Q_1 is forward biased, and the base-collector junction is reverse biased.
- There is current through R_1 and the base-emitter junction of Q_1 to the Low input.

  A Low provides a path to ground for the current. There is no current into the base of Q_2, so it is off.
- The collector of Q_2 is HIGH, thus turning Q_4 on.

  A saturated Q_4 provides a low-resistance path from V_{CC} to the output.

  ∴ HIGH output for a LOW input.
- At the same time, the emitter of Q_2 is at ground potential, keeping Q_3 off.
- Diode D_1 in the TTL circuit prevents negative spikes of voltage on the input from damaging Q_1.
- Diode D_2 ensures that Q_4 will turn off when Q_2 is on (HIGH i/p). The collector voltage of Q_2 is equal to the base-to-emitter voltage, V_{BE} of Q_3 plus the collector-to-emitter voltage, V_{CE}, of Q_2.
- Diode D_2 provides an additional V_{BE} equivalent drop in series with the base-emitter junction of Q_4 to ensure it

turns-off when Q_2 is on.

- The operation of the TTL inverter for the two input states is given below.

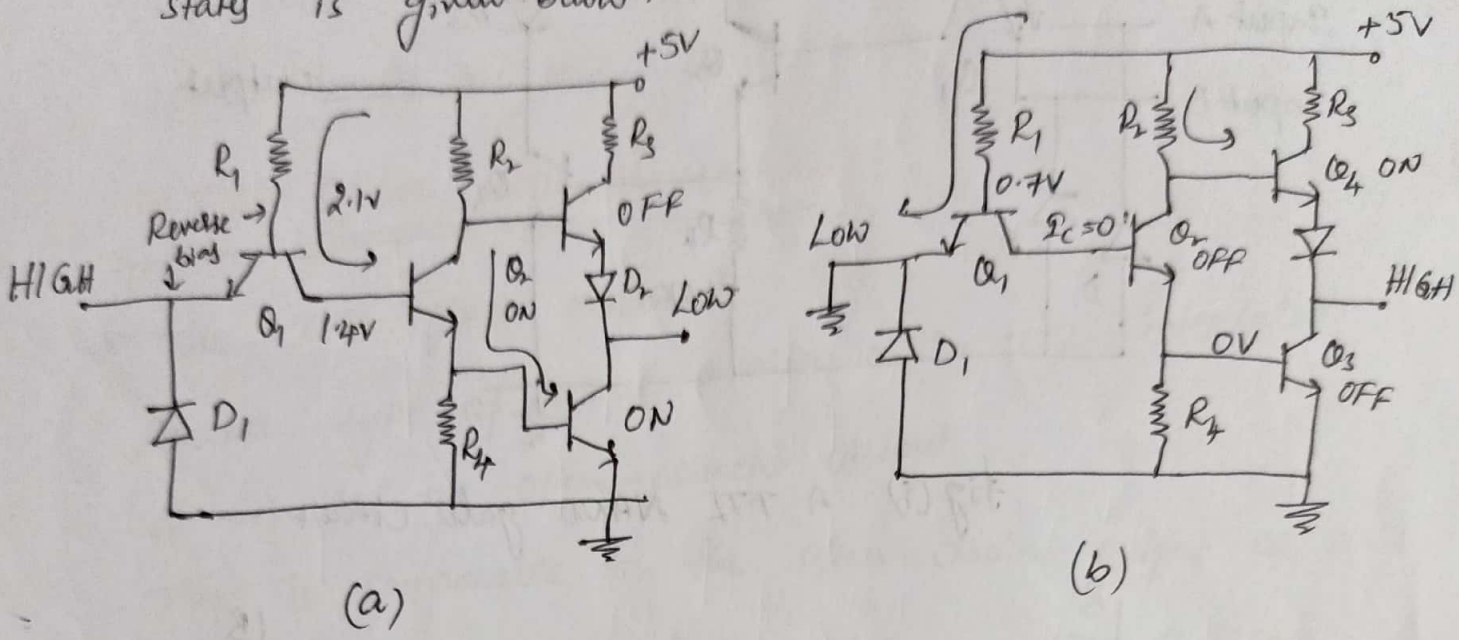


fig. operation of a TTL inverter

- In the circuit in part (a), the base of Q_1 is 2.1V above ground, so Q_2 and Q_3 are on.

In the circuit in part (b), the base of Q_1 is about 0.7V above ground - not enough to turn Q_2 and Q_3 on.

TTL NAND Gate:

- A 2-input TTL NAND gate is shown in fig (i). Basically, it is same as the inverter circuit except for the additional input emitter of Q_1.
- In TTL technology multiple-emitter transistors are used for the input devices. These multiple-emitter transistors can be compared to the diode arrangement as shown in fig (ii)

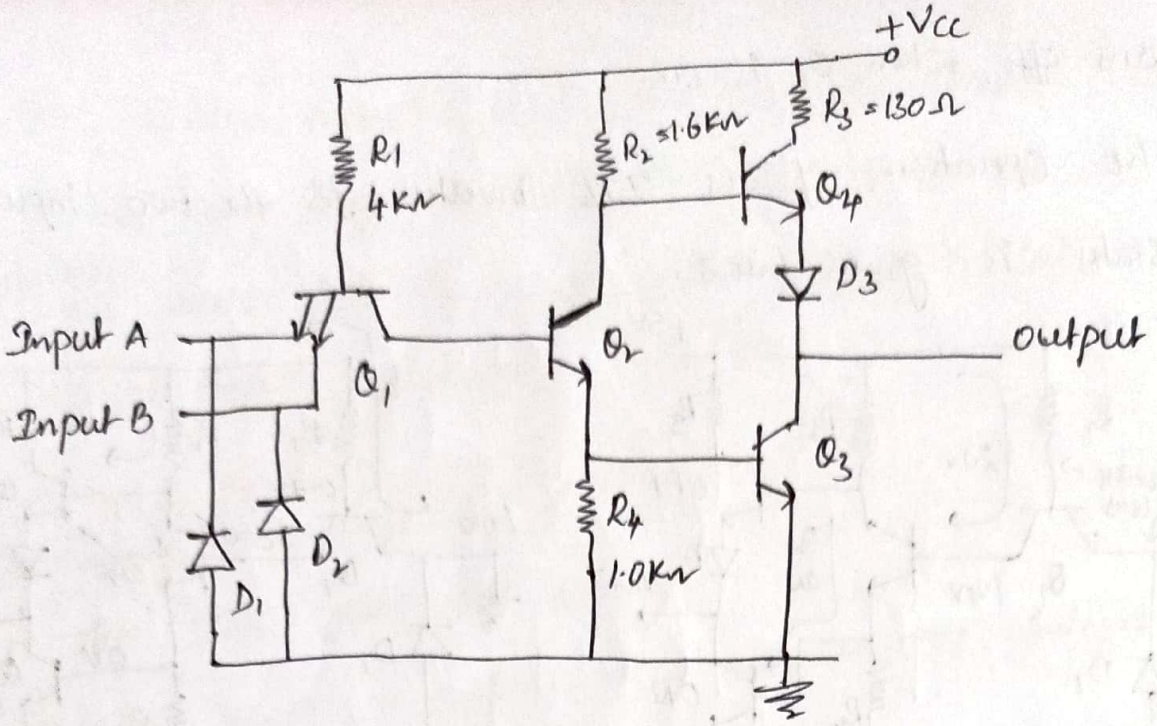


fig (i) A TTL NAND gate circuit

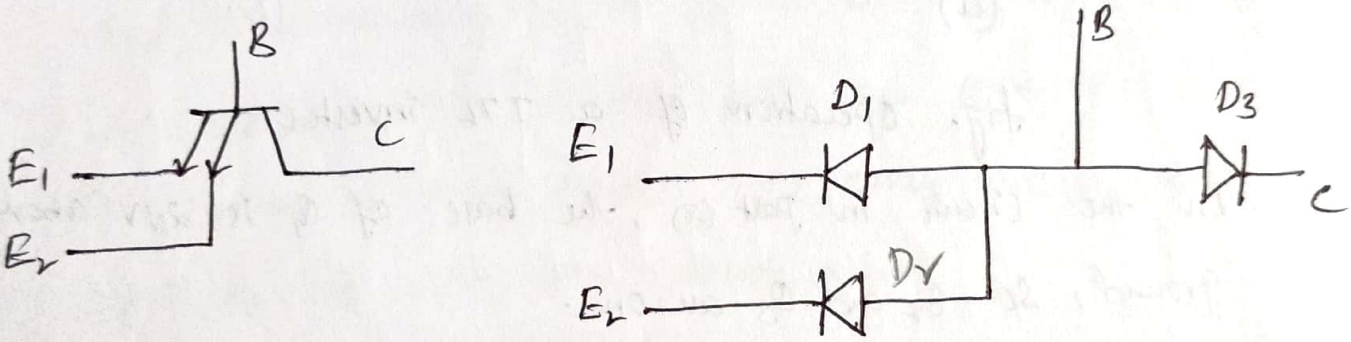


fig (ii) Diode equivalent of a TTL multiple emitter transistor.

. A Low on either input A & input B fowad-biases the respective diode and reverse-biases D_3 (Q_1 base-collector junction).

. This action keeps Q_2 off and results in a HIGH output in the same way as described for the TTL inverter.

. a Low on both inputs will do the same thing

. A HIGH on both inputs reverse-biases both input diodes and fowad-biases D_3 (Q_1 base-collector junction).

. This action turns Q_2 on and results in a Low output in the same way as described for the TTL inverter. This operation of the NAND gate function, i.e the output is Low only if all inputs are HIGH.

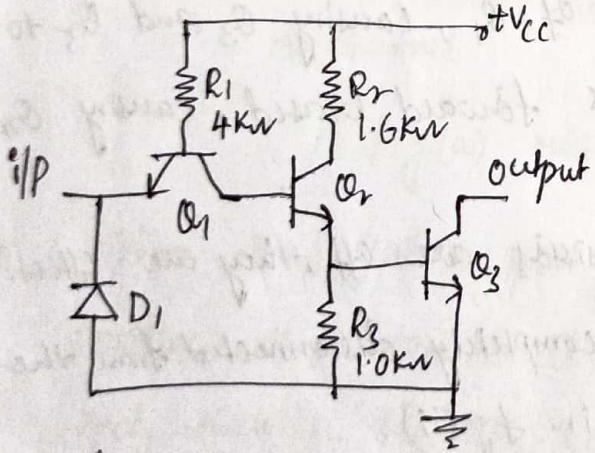
TTL Open-collector outputs:

* The TTL gates described,

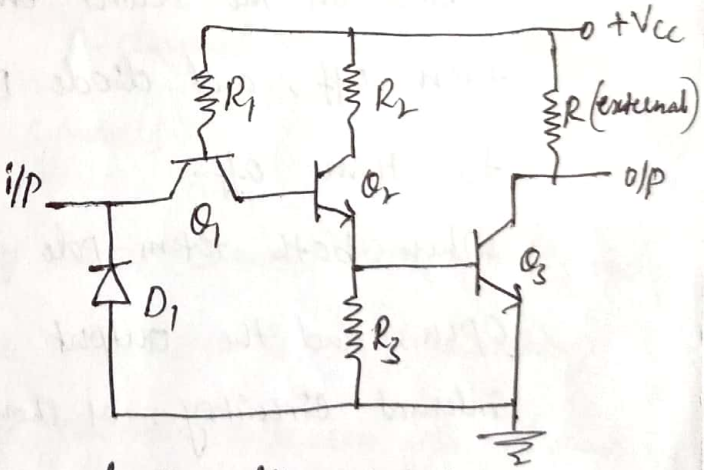
. Another type of output available in TTL integrated circuits is the open-collector output.

. This is comparable to the open-drain output of CMOS.

. A standard TTL inverter with an open collector is shown in below fig(a). The other types of gates are also available with open collector outputs.



fig(a) Open-collector inverter CKt



fig(b) with external pull-up resistor

. The output is the collector of transistor Q_3 with nothing connected to it, hence the name open collector.

. In order to get the proper HIGH and Low logic levels out of the circuit, an external pull-up resistor must be connected

to V_{cc} from the collector of Q_3, as shown in fig (b). When Q_3 is off, the output is pulled up to V_{cc} through the external resistor.

- When Q_3 is on, the output is connected to near-ground through the saturated transistor.

Tristate TTL gates:

- The below fig (i) shows the basic circuit for a TTL tristate inverter.
- When the enable input is Low, Q_2 is off, and the output circuit operates as a normal totem-pole configuration, in which the output state depends on the input state.
- When the enable input is HIGH, Q_2 is on. There is thus a Low on the second emitter of Q_1, causing Q_3 and Q_5 to turn off, and diode D_1 is forward biased, causing Q_4 also to turn off.
- When both totem-pole transistors are off, they are effectively open, and the output is completely disconnected from the internal circuitry, as shown in fig (ii).

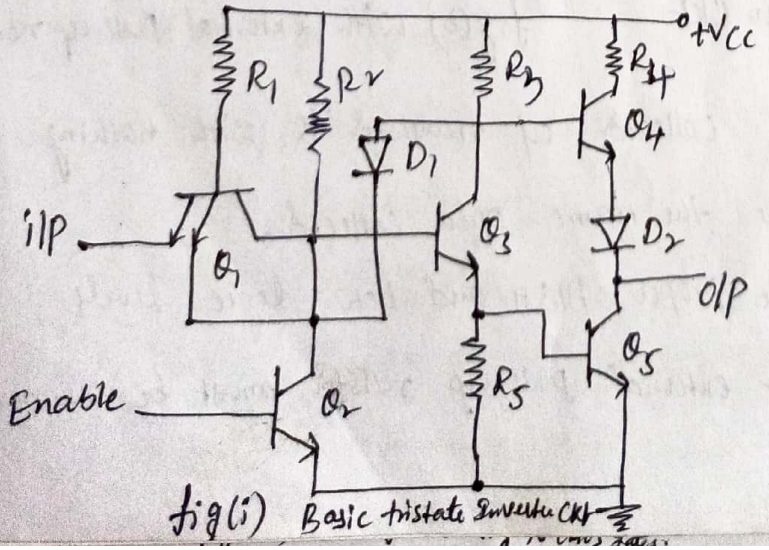


fig (i) Basic tristate inverter ckt

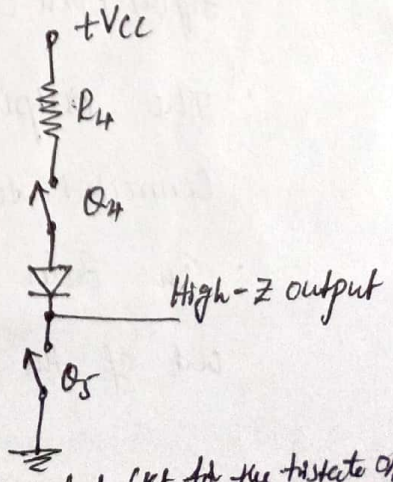


fig (ii) Equivalent ckt for the tristate o/p in the high Z state

CMOS Circuits:

MOSFET:

- Metal-oxide semiconductor field-effect transistors (MOSFETs) are the active switching elements in CMOS circuits.
- These devices differ greatly in construction and internal operation from bipolar junction transistors used in TTL circuits, but the switching action is basically the same: they function ideally as open & closed switches, depending on the input.
- The fig (a) shows the symbols for both n-channel and P-channel MOSFETs.

fig (a) MOSFET symbols

- When the gate voltage of an n-channel MOSFET is more positive than the source, the MOSFET is on (saturation), and there is, ideally, a closed switch between the drain and the source.
- When the gate-to-source voltage is zero, the MOSFET is off (cutoff), and there is, ideally, an open switch between the drain and the source as shown in fig (b).

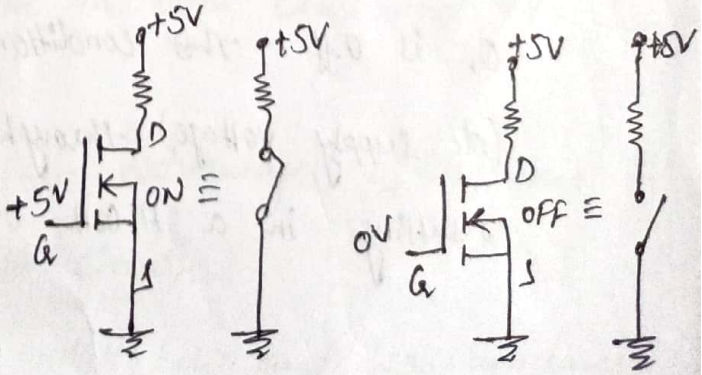


fig (b) n-channel switch

CMOS Inverter :

- Complementary MOS (CMOS) logic uses the MOSFET in complementary pairs as its basic element.
- A complementary pair uses both P-channel and n-channel enhancement MOSFETs, as shown in the inverter circuit below

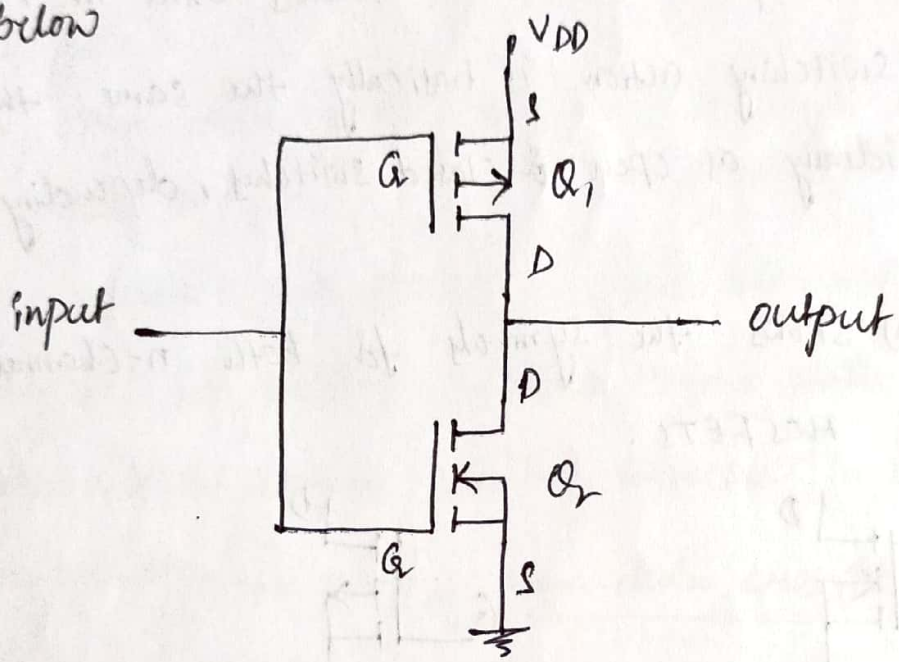


fig. CMOS inverter circuit

- When a HIGH is applied to the input, the P-channel MOSFET Q_1 is off and the n-channel MOSFET Q_2 is on. This condition connects the output to ground through the on resistance of Q_2, resulting in a Low output.
- When a Low is applied to the input, as Q_1 is on and Q_2 is off. This condition connects the output to $+V_{DD}$ (dc supply voltage) through the on resistance of Q_1, resulting in a HIGH output.

CMOS Open-Drain gates:

- The term open-drain means that the drain terminal of the output transistor is unconnected and must be connected externally to V_{DD} through a load.
- An open-drain gate is the CMOS counterpart of an open-collector TTL gate.
- An open-drain output circuit is a single n-channel MOSFET as shown in fig (a).
- An external pull-up resistor must be used, as shown in part (b), to produce a HIGH output state.
- open-drain outputs can be connected in a wired-AND configuration.

fig. Open-drain CMOS gate

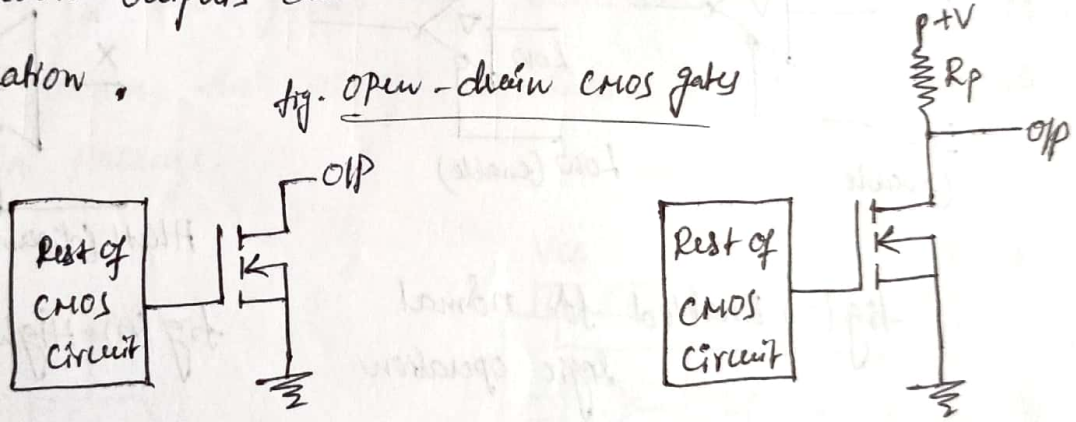


fig (a) unconnected O/P fig(b) with pull-up resistor

Tristate CMOS gates:

- Tristate outputs are available in both CMOS and TTL logic.
- The tristate output combines the advantages of the totem-pole and open-collector circuits.
- The three output states are HIGH, LOW and high-impedance (high-Z)

- When selected for normal logic-level operation, as determined by the state of the enable input, a tristate circuit operates in the same way as a regular gate.
- When a tristate circuit is selected for high-Z operation, the output is effectively disconnected from the rest of the circuit by the internal circuitry.
- The below figure illustrates the operation of a tristate circuit. The inverted triangle (▽) designates a tristate output.

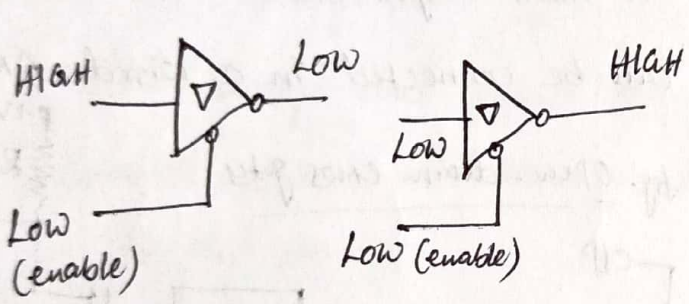


fig (a) Enabled for normal logic operation

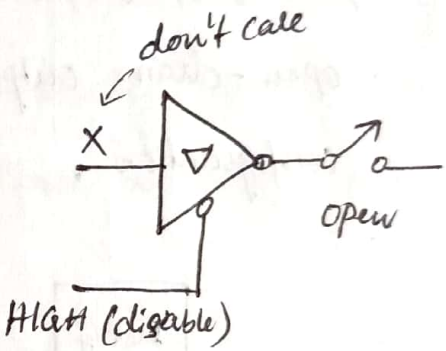


fig (b) High-Z state

- The circuitry in a tristate CMOS gate, as shown in fig (c), allows each of the output transistors Q_1 and Q_2 to be turned off at the same time, thus disconnecting the output from the rest of the circuit.
- When the enable input is LOW, the device is enabled for normal logic operation. When the enable is High, both Q_1 and Q_2 are off, and the ckt is in the high-Z state.

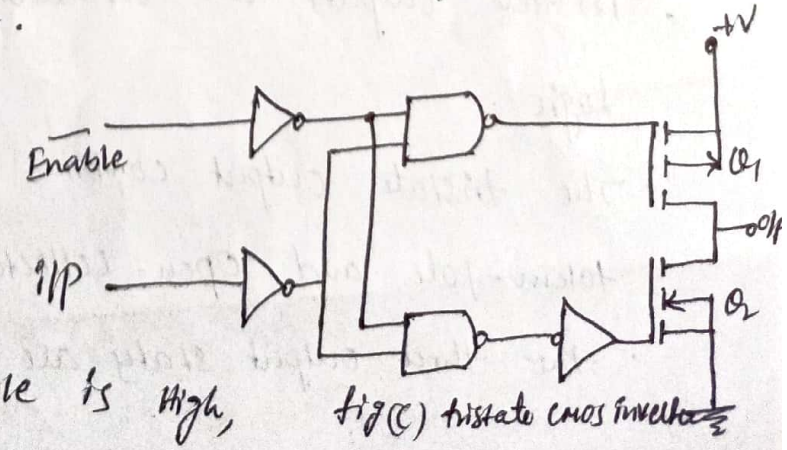
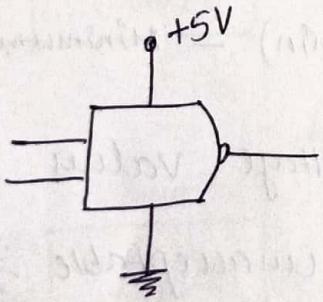


fig (c) tristate CMOS inverter

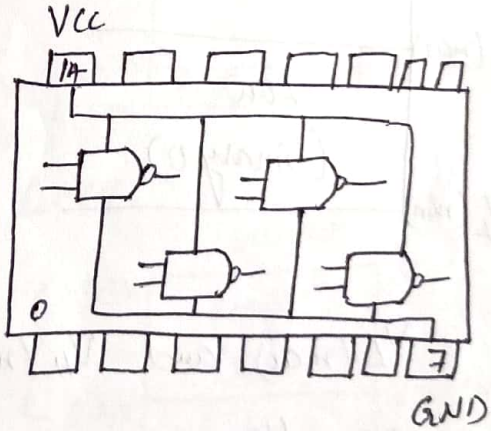
→ Basic operational characteristics and parameters :

• DC supply voltage :

- The nominal value of the dc supply voltage for TTL devices is +5V.
- TTL is also designated as T^2L.
- CMOS devices are available in different supply voltage categories : +5V, 3.3V
- The dc supply voltage is connected to the Vcc pin of an IC package, and ground is connected to the GND pin.
- Both voltage and ground are distributed internally to all elements within the package, as shown in below figure for a 14-pin package.



(a) Single gate



(b) IC dual in-line package

• Logic levels :

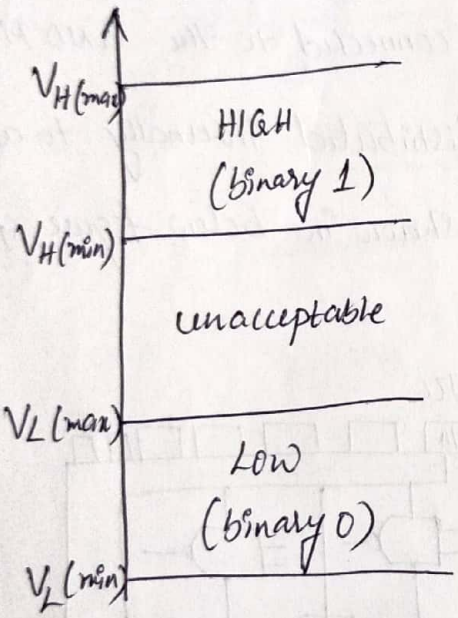
- ~~CMOS logic levels~~ The voltages used to represent a 1 and a 0 are called logic levels.
- Ideally, one voltage level represents a HIGH and another

voltage level represents a LOW.

- In a practical digital circuit, a HIGH can be any voltage between a specified minimum value and a specified maximum value. Similarly a LOW can be any voltage between a specified minimum and a specified maximum.

There can be no overlap between the accepted range of HIGH levels and the accepted range of LOW levels.

- The below figure illustrates the general range of LOWs and HIGHs for a digital circuit.



- Here $V_{H(max)}$ represents the maximum HIGH voltage value

$V_{H(min)}$ – minimum HIGH voltage value

$V_{L(max)}$ – maximum LOW voltage value

$V_{L(min)}$ – minimum LOW voltage value

. The voltage values between $V_{L(max)}$ and $V_{H(min)}$ are unacceptable for proper operation. A voltage in the unacceptable range can appear as either a HIGH or a LOW to a given circuit.

CMOS Logic Levels:

There are four different logic level specifications:

V_{IL}, V_{IH}, V_{OL} and V_{OH}.

- For CMOS circuits, the ranges of input voltages (V_{IL}) that can represent a valid Low (logic 0) are from 0V to 1.5V for the 5V logic and 0V to 0.8V for the 3.3V logic.
- The ranges of input voltages (V_{IH}) that can represent a valid HIGH (logic 1) are from 3.5V to 5V for the 5V logic and 2V to 3.3V for the 3.3V logic as indicated in below figures (a, b)

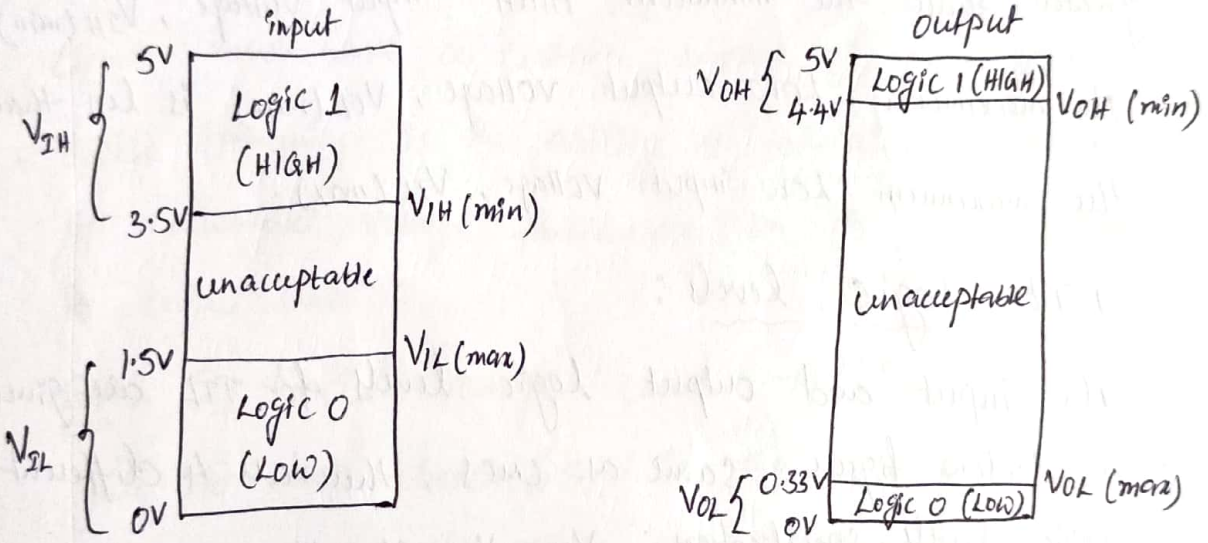


fig (a) +5V CMOS

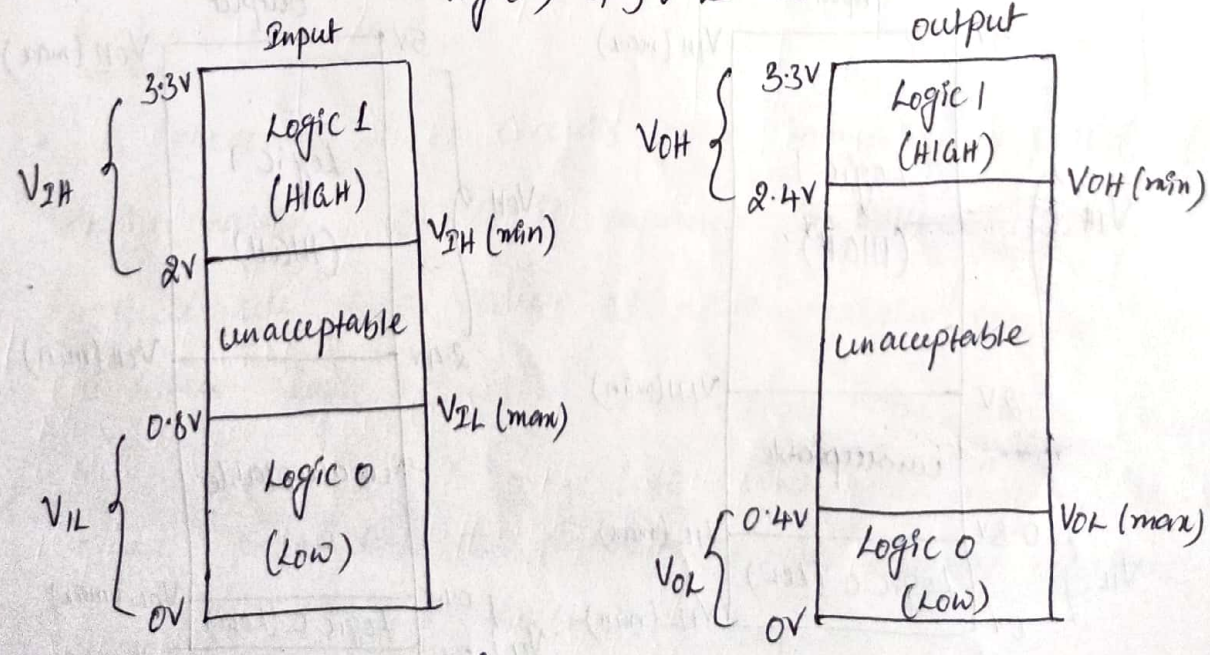


fig (b) +3.3V CMOS

The ranges of values from 1.5V to 3.5V for 5V logic and 0.8V to 2V for 3.3V logic are regions of unpredictable performance, and values in these ranges are unacceptable.

- When the an input voltage is in one of these ranges, it can be interpreted as either a HIGH & a LOW by the logic circuit.

∴ CMOS gates cannot be operated reliably when the input voltages are in these unacceptable ranges.

NOTE: The minimum HIGH output voltage, $V_{OH}(min)$, is greater than the minimum HIGH input voltage, $V_{IH}(min)$. The maximum LOW output voltage, $V_{OL}(max)$ is less than the maximum LOW input voltage, $V_{IL}(max)$.

TTL Logic levels:

- The input and output logic levels for TTL are given in below figure. Same as CMOS, there are 4 different logic levels specifications: V_{IL}, V_{IH}, V_{OL}, V_{OH}.

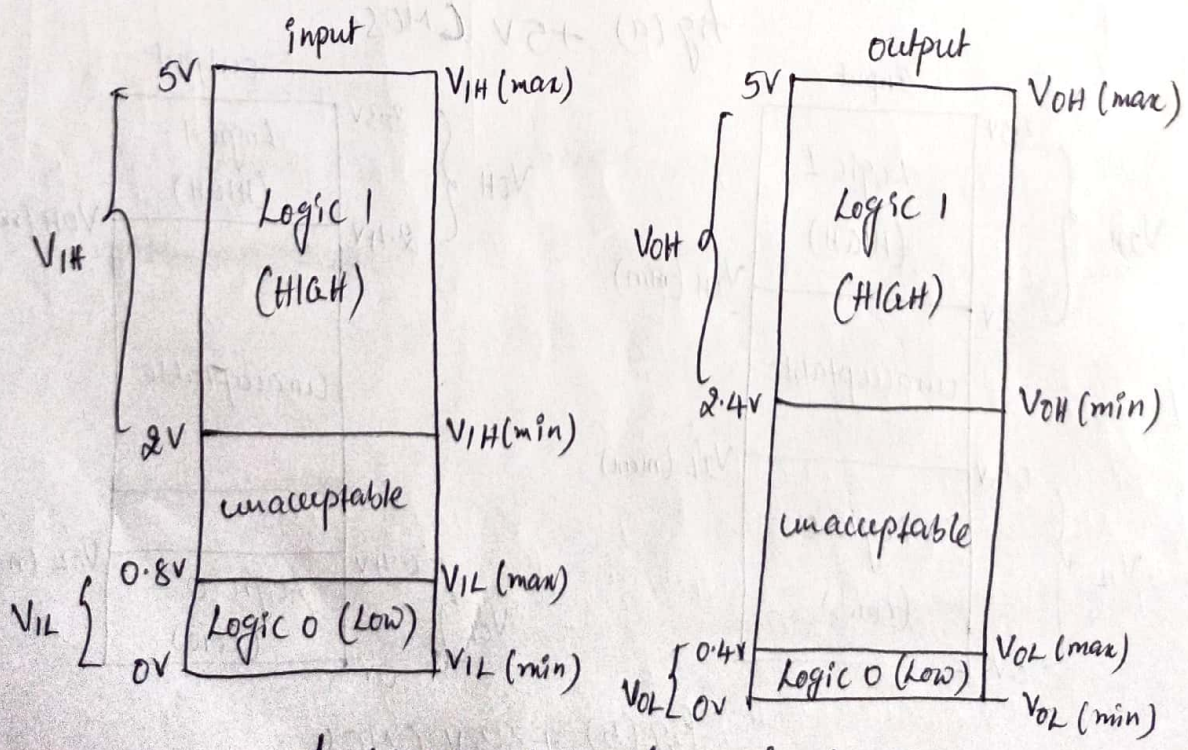


fig (c) i/p and o/p logic levels for TTL

Noise Immunity :

- Noise is unwanted voltage that is induced in electrical circuits.
- Wires and other conductors within a system can pick up stray high-frequency electromagnetic radiation from adjacent conductors in which currents are changing rapidly & from many other sources external to the system. Also power-line voltage fluctuation is a form of low frequency noise.
- In order not to be adversely affected by noise, a logic circuit must have a certain amount of noise immunity.
- Noise immunity is the ability to tolerate a certain amount of unwanted voltage fluctuation on its inputs without changing its output state.

  Ex: If noise voltage causes the input of a 5V CMOS gate to drop below 3.5 V in the HIGH state, the input is in the unacceptable region and operation is unpredictable.

Noise Margin :

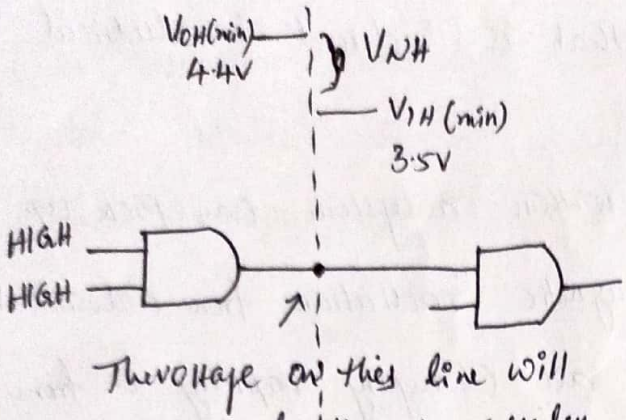
- A measure of a circuit's noise immunity is called the noise margin, which is expressed in volts.
- There are two values of noise margin specified for a given logic circuit: HIGH-level noise margin (V_{NH})
  LOW-level noise margin (V_{NL})

These parameters are defined by the following equations:

$$V_{NH} = V_{OH(min)} - V_{IH(min)}$$

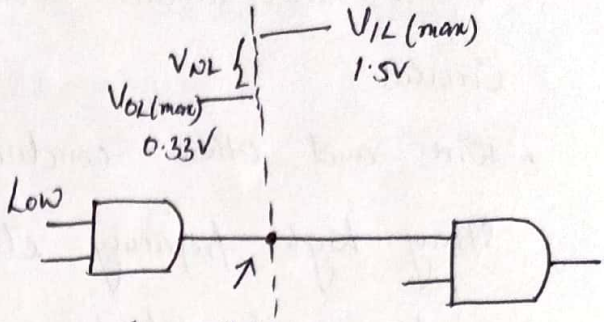
$$V_{NL} = V_{IL(max)} - V_{OL(max)}$$

- Sometimes the noise margin expressed as a percentage of V_{CC}.



The voltage on this line will never be less than 4.4V unless noise & improper operation is introduced.

fig (a) HIGH-level noise margin

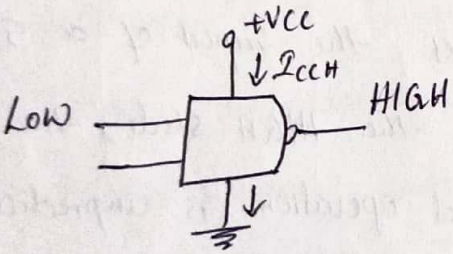


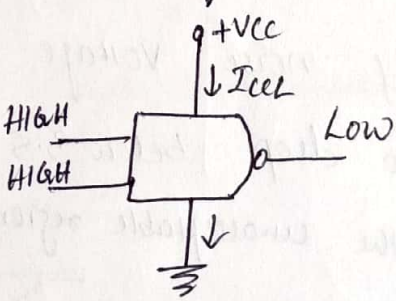
The voltage on this line will never exceed 0.33V unless noise & improper operation is introduced.

fig (b). Low-level noise margin

• Power Dissipation (P_D):

- A Logic gate draws current from the dc supply voltage source as indicated in below fig.





(a)

- When the gate is in the HIGH output state, an amount of current designated by I_{CCH} is drawn, and in the Low output state, a different amount of current, I_{CCL} is drawn.

Ex: If I_{CCH} is specified as 1.5mA when V_{CC} is 5V and if the gate is in a static (non changing) HIGH output state, the Power dissipation (P_D) of the gate is

$$P_D = V_{CC} I_{CCH} = (5)(1.5m) = 7.5mW$$

- When a gate is pulsed, its output switches back and forth between HIGH and LOW, and the amount of supply current varies between I_{CCH} and I_{CCL}.
- The average supply current is

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2}$$

The average power dissipation is

$$P_D = V_{CC} I_{CC}$$

- The power dissipation in a TTL circuit is essentially constant over its range of operating frequency.
  Power dissipation in CMOS, however, is frequency dependent. It is extremely low under static (dc) conditions and increases as the frequency increases.
- These characteristics are shown in the general curves of below figure.

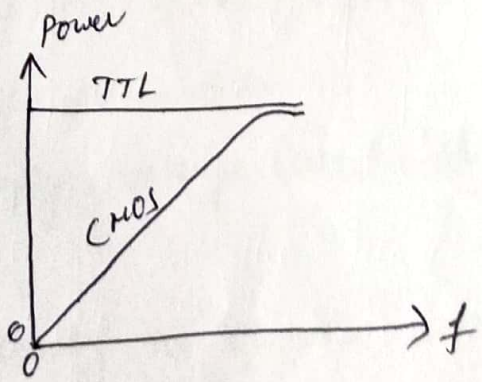
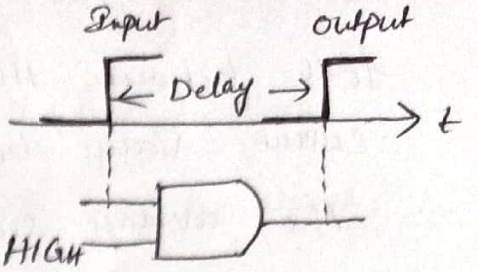


fig. Power Vs frequency curves for TTL and CMOS

- **Propagation Delay time (tp):**
- When a signal passes (propagates) through a logic circuit, it always experiences a time delay shown in below fig.
- A change in the output level always occurs a short time,

called the propagation delay time.



- It is the amount of time that it takes for a change in the input signal to produce a change in the output signal.

- There are two propagation delay times specified for logic gates.
  - t_{PHL}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from HIGH to LOW.
  - t_{PLH}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from LOW to HIGH.

→ IC Interfacing (& Interfacing CMOS and TTL):

- To achieve optimum performance in a digital system, devices from more than one logic family can be used, taking advantages of the superior characteristics of each family for different parts of the system.

  Ex: CMOS logic ICs can be used in those parts of the system where low power dissipation is required, while TTL can be used in those portions of the system which requires high speed of operation.

- Therefore, it is necessary to examine the interface between TTL and CMOS devices.
- The 74C series of CMOS ICs can be operated for any supply voltage in the range of 3V to 15V, whereas the 74HC/74HCT/74AC/74ACT series have the supply voltage range of 2V to 6V.
- Since the supply voltage used for all 74 series TTL ICs is 5V.

  ∴ It is necessary to operate CMOS devices at +5V, to make it compatible with TTL devices.

CMOS Driving TTL:

- The fig(i) shows a CMOS gate driving N TTL gates.
- For such an arrangement to operate properly the

~~following~~

following conditions are required to be satisfied,

$V_{OH}(CMOS) \geq V_{IH}(TTL) \rightarrow (1)$

$V_{OL}(CMOS) \leq V_{IL}(TTL) \rightarrow (2)$

$-I_{OH}(CMOS) \geq N I_{IH}(TTL) \rightarrow (3)$

$I_{OL}(CMOS) \geq -N I_{IL}(TTL) \rightarrow (4)$

V_{IH} – High level i/p voltage (logic 1)

V_{IL} – Low level i/p voltage (logic 0)

V_{OH} – High level o/p voltage (Logic 1)

V_{OL} – Low level o/p voltage (logic 0)

I_{OH} – High level o/p current (1 level)

I_{IH} – High level i/p current 1 level

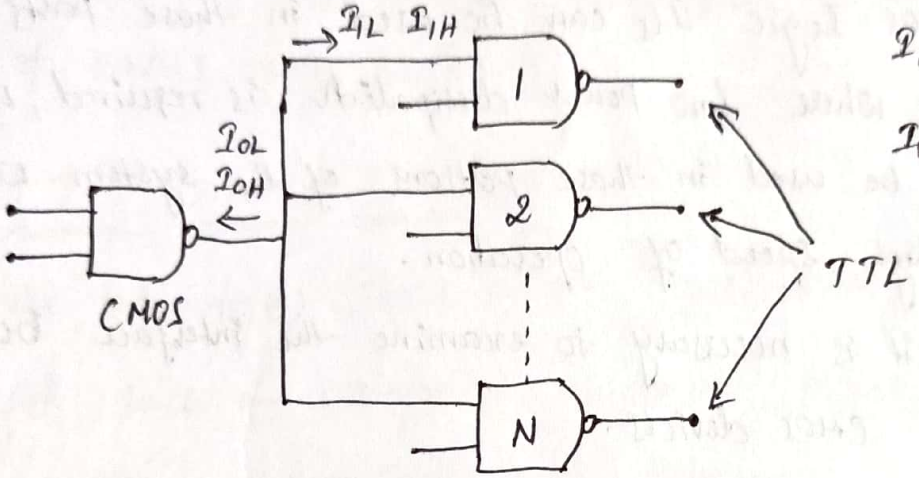


fig (i) CMOS gate driving N TTL gates

i) The conditions of equations (1) & (2) are always satisfied.

Ex: The noise margins when 74ACT (CMOS) is driving 74ALS (TTL) gates are

$\Delta 1 = 3.76 - 2.0 = 1.76\,V$ ← (from the specifications given in CMOS & TTL standard tables)

$\Delta 0 = 0.8 - 0.37 = 0.43\,V$

ii) The conditions of equations (3) & (4) are always satisfied for 74HC/74HCT/74AC/74ACT series. The value of N is different for different series.

The value of N when 74ACT is driving 74ALS gates is 240.

In case of 74C series, the condition of eqn (3) is satisfied for small values of N but the condition of

equation (4) is not satisfied even for N=1, except in case of 74L and 74ALS TTL series. This difficulty can be overcome by using CMOS buffers having an adequate available output current.

· If 74C series gate is driving 74L series gate, the condition of equ" (4) is satisfied for N=2 and in case of 74ALS gates for N=3.

TTL Driving CMOS :

. The below fig (a) shows a TTL gate driving N CMOS gates.

. For such an arrangement to operate properly, the following conditions are required to be satisfied:

$$V_{OH}(TTL) \geq V_{IH}(CMOS) \rightarrow (5)$$

$$V_{OL}(TTL) \leq V_{IH}(CMOS) \rightarrow (6)$$

$$-I_{OH}(TTL) \geq N I_{IH}(CMOS) \rightarrow (7)$$

$$I_{OL}(TTL) \geq -N I_{IL}(CMOS) \rightarrow (8)$$

. All the above conditions are always satisfied in case of 74HCT and 74ACT series for high values of N. This shows that these two CMOS series are TTL compatible.

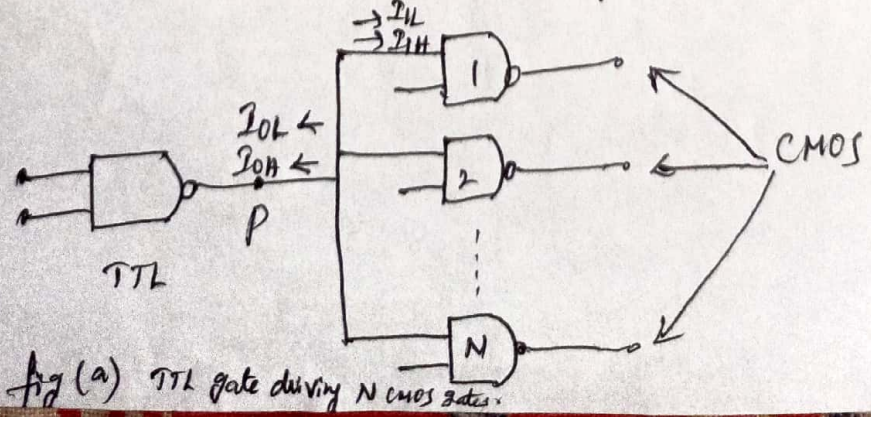


fig (a) TTL gate driving N CMOS gates.

. In the case of 74C/74HC/74AC series, the condition of eqn (5) is not satisfied.

. A circuit modification used to raise V_{OH} (TTL) above 3.5V is obtained by connecting a resistance ($\simeq$ 2kΩ) between points P and V_{cc} as shown in fig (b). This acts as a passive pull-up, which pulls up the voltage at P, by charging the capacitor Co present between P and the ground terminal, to a higher value ($\simeq V_{cc}$) after the transistor T_4 of the TTL becomes non-conducting.

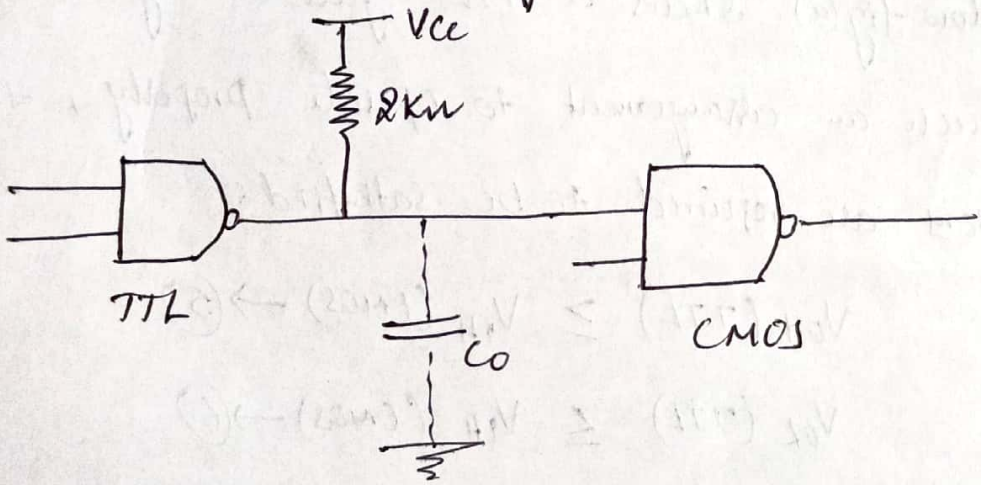


fig (b) Circuit to pull up the output voltage of TTL.