6.3.11 Shift Register Counters

One of the applications of shift registers is that they can be arranged to form several types of counters. Shift register counters are obtained from serial-in, serial-out shift registers by providing feedback from the output of the last FF to the input of the first FF. These devices are called counters because they exhibit a specified sequence of states. The most widely used shift register counter is the ring counter (also called the basic ring counter or the simple ring counter) as well as the twisted ring counter (also called the Johnson counter or the switch-tail ring counter).

Ring counter: This is the simplest shift register counter. The basic ring counter using D FFs is shown in Figure 6.94. The realization of this counter using J-K FFs is shown in Figure 6.95. Its state diagram and the sequence table are shown in Figure 6.96. Its timing diagram is shown in Figure 6.97. The FFs are arranged as in a normal shift register, i.e. the Q output of each stage is connected to the D input of the next stage, but the Q output of the last FF is connected back to the D input of the first FF such that the array of FFs is arranged in a ring and, therefore, the name *ring counter.*

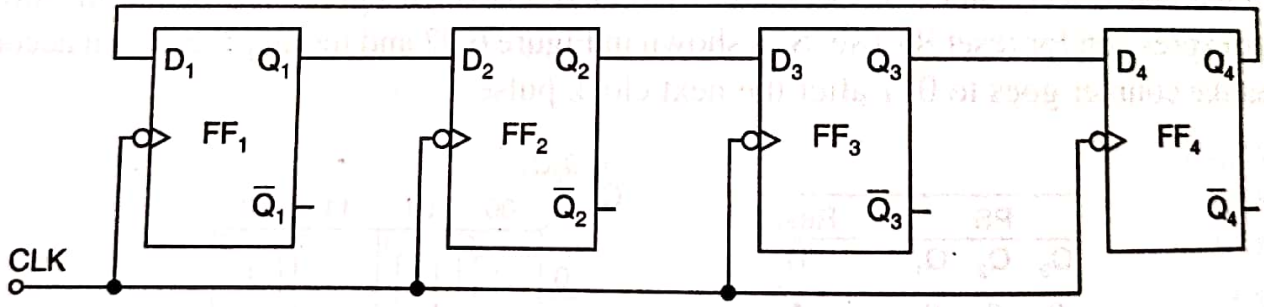


Figure 6.94 Logic diagram of a 4-bit ring counter using D flip-flops.

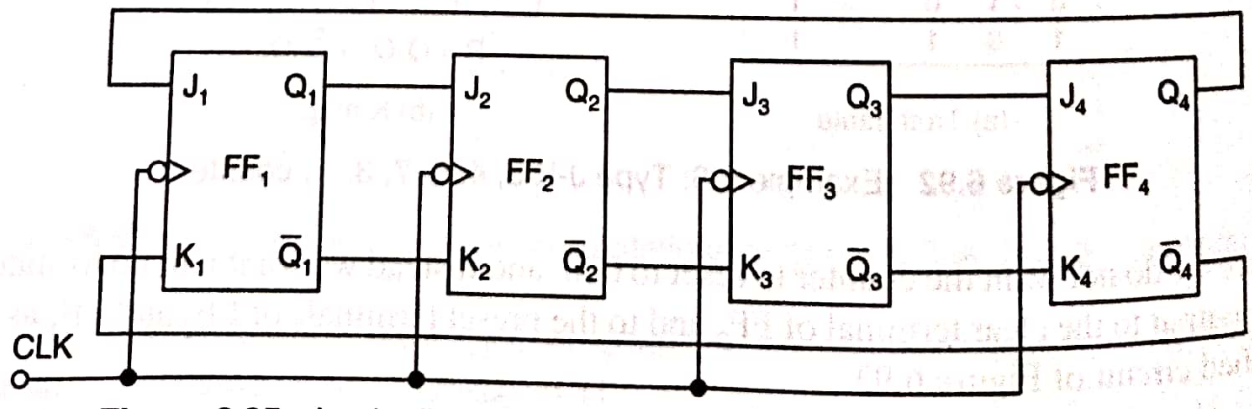
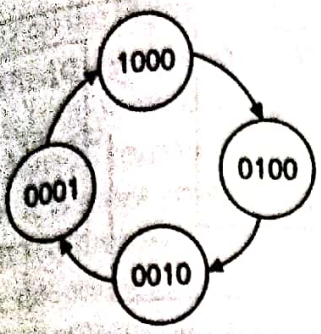


Figure 6.95 Logic diagram of a 4-bit ring counter using J-K flip-flops.



(a) State diagram

Q_1	Q_2	Q_3	Q_4	After clock pulse
1	0	0	0	0
0	1	0	0	1
0	0	1	0	2
0	0	0	1	3
1	0	0	0	4
0	1	0	0	5
0	0	1	0	6
0	0	0	1	7

(b) Sequence table

Figure 6.96 State diagram and sequence table of a 4-bit ring counter.

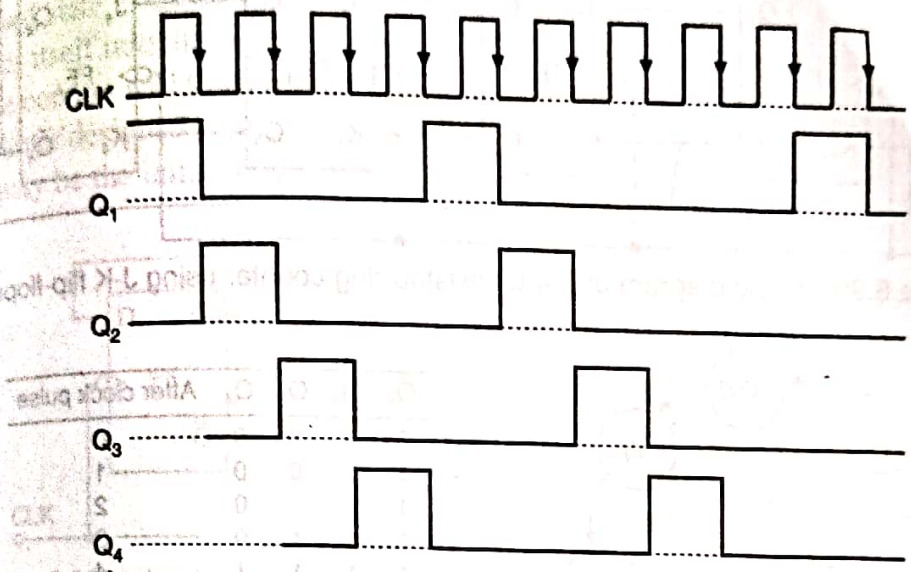


Figure 6.97 Timing diagram of a 4-bit ring counter.

In most instances, only a single 1 is in the register and is made to circulate around the register as long as clock pulses are applied. Initially, the first FF is preset to a 1. So, the initial state is 1000, i.e. $Q_1 = 1, Q_2 = 0, Q_3 = 0$ and $Q_4 = 0$. After each clock pulse, the contents of the register are shifted to the right by one bit and Q_4 is shifted back to Q_1. The sequence repeats after four clock pulses. The number of distinct states in the ring counter, i.e. the mod of the ring counter is equal to the number of FFs used in the counter. An n-bit ring counter can count only n bits, whereas an n-bit ripple counter can count 2^n bits. So, the ring counter is uneconomical compared to a ripple counter, but has the advantage of requiring no decoder, since we can read the count by simply noting which FF is set. Since it is entirely a synchronous operation and requires no gates external to FFs, it has the further advantage of being very fast.

Twisted ring counter (Johnson counter): This counter is obtained from a serial-in, serial-out shift register by providing feedback from the inverted output of the last FF to the D input of the first FF. The Q output of each stage is connected to the D input of the next stage, but the $\overline{Q}$ output of the last stage is connected to the D input of first stage, therefore, the name *twisted ring counter*. This feedback arrangement produces a unique sequence of states.

The logic diagram of a 4-bit Johnson counter using D FFs is shown in Figure 6.98. The realization of the same using J-K FFs is shown in Figure 6.99. The state diagram and the sequence table are shown in Figure 6.100. The timing diagram of a Johnson counter is shown in Figure 6.101.

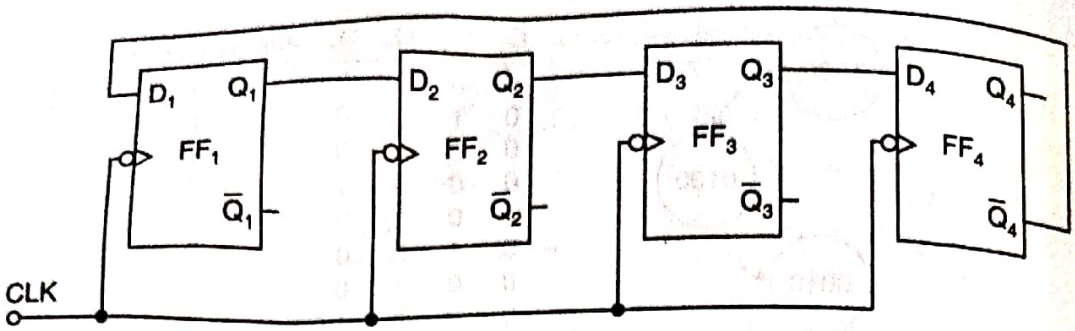


Figure 6.98 Logic diagram of a 4-bit twisted ring counter using D flip-flops.

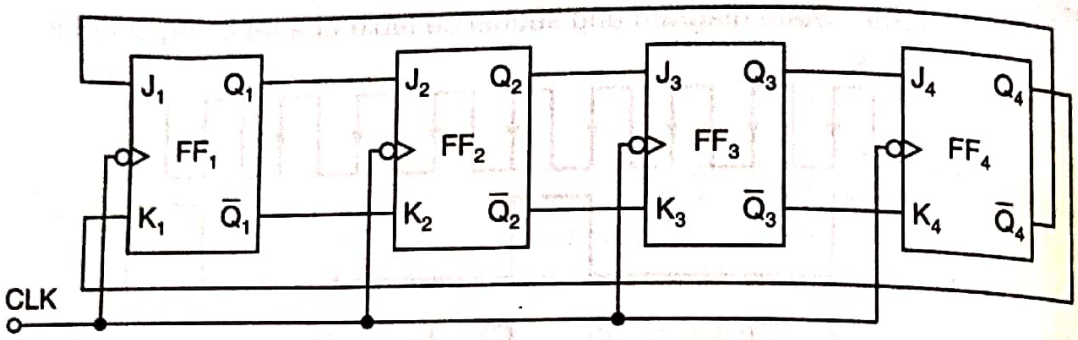
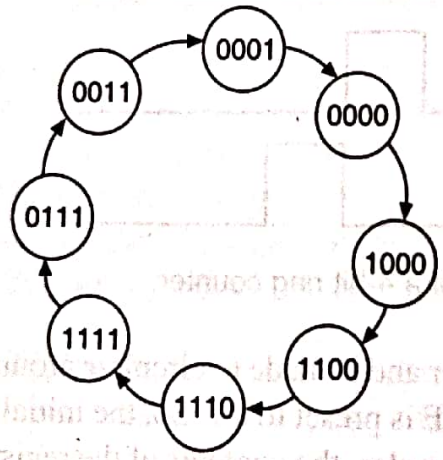


Figure 6.99 Logic diagram of a 4-bit twisted ring counter using J-K flip-flops.



(a) State diagram

Q_1	Q_2	Q_3	Q_4	After clock pulse
0	0	0	0	0
1	0	0	0	1
1	1	0	0	2
1	1	1	0	3
1	1	1	1	4
0	1	1	1	5
0	0	1	1	6
0	0	0	1	7
0	0	0	0	8
1	0	0	0	9

(b) Sequence table

Figure 6.100 State diagram and sequence table of a twisted ring counter.

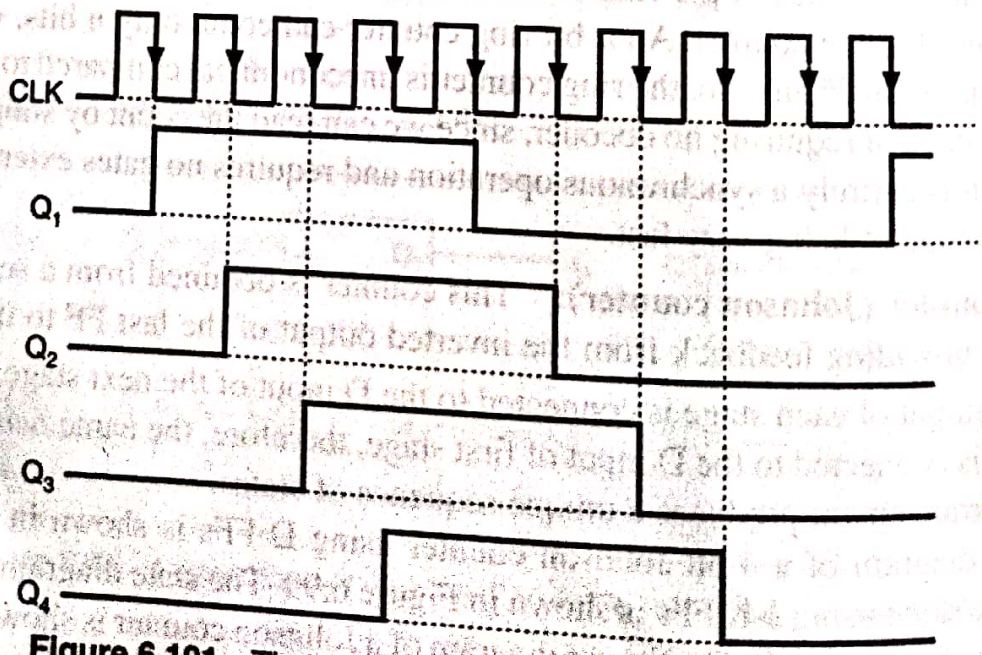


Figure 6.101 Timing diagram of a 4-bit twisted ring counter.

Let initially all the FFs be reset, i.e. the state of the counter be 0000. After each clock pulse, the level of Q_1 is shifted to Q_2, the level of Q_2 to Q_3, Q_3 to Q_4 and the level of $\bar{Q}_4$ to Q_1 and the sequence given in Figure 6.100b is obtained. This sequence is repeated after every eight clock pulses.

An n FF Johnson counter can have $2n$ unique states and can count up to $2n$ pulses. So, it is a mod-$2n$ counter. It is more economical than the normal ring counter, but less economical than the ripple counter. It requires two input gates for decoding regardless of the size of the counter. Thus, it requires more decoding circuitry than that by the normal ring counter, but less than that by the ripple counter. It represents a middle ground between the ring counter and the ripple counter.

Both types of ring counters suffer from the problem of lock-out, i.e. if the counter finds itself in an unused state, it will persist in moving from one unused state to another and will never find its way to a used state. This difficulty can be corrected by adding a gate. With this addition, if the counter finds itself initially in an unused state, then after a number of clock pulses, depending on the state, the counter will find its way to a used state and thereafter, follow the desired sequence. A Johnson counter designed to prevent lock-out is shown in Figure 6.102. A self-starting ring counter (whatever may be the initial state, single 1 will eventually circulate) is shown in Figure 6.103.

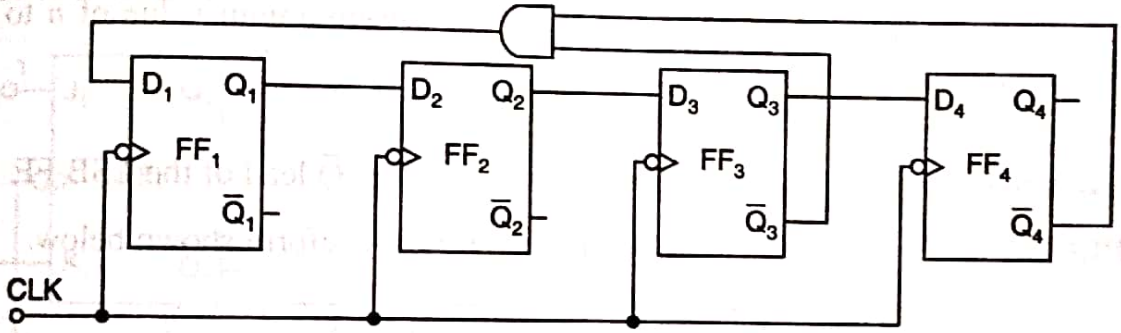


Figure 6.102 Logic diagram of a 4-bit Johnson counter designed to prevent lock-out.

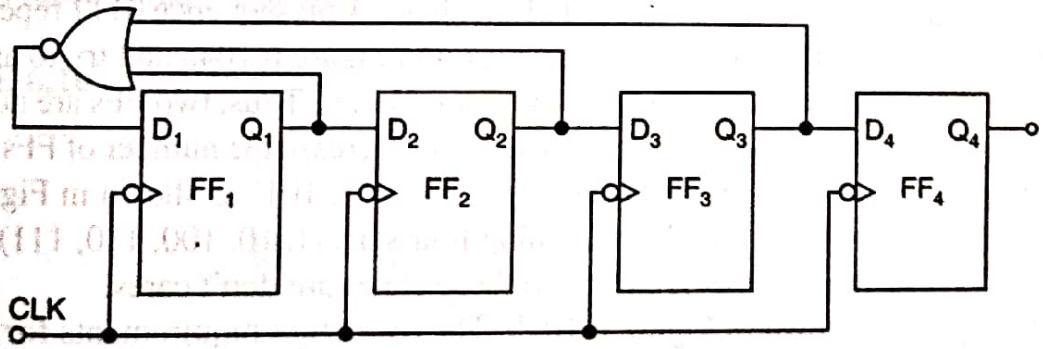


Figure 6.103 Logic diagram of a self-starting ring counter.