$$\Rightarrow \frac{I_{C2}}{I_{C1}} - 1 = \left(\frac{\beta_2}{\beta_1} - 1\right) \frac{R_b + R_e}{R_b + R_e(1+\beta_2)}$$

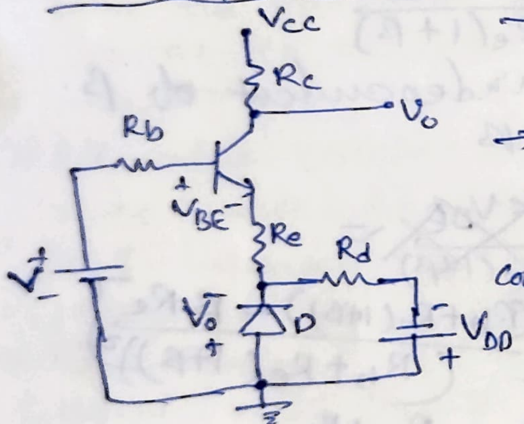
$$\Rightarrow S'' = \frac{\Delta I_C}{\Delta \beta} = \frac{I_{C1}\, S_2}{\beta_1 (1+\beta_2)}$$ where S_2 is the value of stabilizing factor S when $\beta = \beta_2$

- Minimizing S also minimizes S''. This means that the ratio R_b/R_e must be small.
- In order to keep S' small, a large R_b or R_e is required
- In all cases, it is desirable to use as large an emitter resistance R_e as practical, & compromise will usually be necessary for selection of R_b

→ **Bias Compensation**

- If loss in signal gain is intolerable in a particular application, it is possible to use compensating techniques to reduce the drift of operating point.

↳ **Diode Compensation for V_{BE}**



- The diode is kept biased in forward direction by source V_{DD} & resistance R_d.
- If the diode is of same material & type as transistor, the voltage V_o across diode will have same temp. coeff. ($-2.5\ mV/°C$) as base-to-emitter voltage V_{BE}
- If we write KVL around base ckt

$$-V + I_B R_b + V_{BE} + (I_C + I_B) R_e - V_o = 0$$

$$\Rightarrow I_B = \frac{V + V_o - V_{BE} - I_C R_e}{R_e + R_b}$$

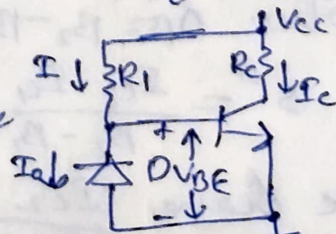
$$\rightarrow I_C = (1+\beta) I_{CO} + \beta I_B = (1+\beta) I_{CO} + \beta \frac{(V + V_o - V_{BE} - I_C R_e)}{R_e + R_b}$$

$$\Rightarrow I_C [R_b + R_e(1+\beta)] = (1+\beta)(R_e + R_b) I_{CO} + \beta[V - (V_{BE} - V_o)]$$

$$\Rightarrow I_C = \frac{\beta[V - (V_{BE} - V_o)] + (R_e + R_b)(\beta+1) I_{CO}}{R_b + R_e(1+\beta)}$$

- Since V_{BE} tracks V_o w.r.t temp., I_C will be insensitive to variations in V_{BE}

↳ **Diode Compensation for I_{CO}**



- If diode & transistor are of same type & material, the reverse saturation current I_o of diode will increase with temp. at same rate as transistor collector saturation current I_{CO}

Thermal Runaway

→ The max. average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction & may lie in the range from a few milliwatts to 200W

→ This max. power is limited by temp. that collector-to-base junction can withstand. for Si transistors this temp. is in range 150°C to 225°C, & for Ge it is b/w 60°C & 100°C

→ The junction temp. may rise either because ambient temp. or because of self-heating.

→ The max. power dissipation is usually specified for transistor enclosure (case) or ambient temp. of 25°C

→ The problem of self heating results from power dissipated at the collector junction.

→ As a consequence of junction power dissipation, junction temp. rises & this in turn increases collector current, with subsequent increase in power dissipation. This phenomenon is reffered to as thermal runaway

→ If this thermal runaway continues, it may result in permanently damaging the transistor.

Thermal Resistance

→ The steady-state temp. rise at collector junction is proportional to power dissipated at the junction

$$\Delta T = T_j - T_A = \Theta P_D$$

where T_j & T_A are junction & ambient temp.s respectively in degree centigrade, & P_D is power in watts dissipated at collector junction.

→ The const. of proportionality Θ is called thermal resistance. Its value depends on size of transistor, on convection or radiation to the surroundings, on forced-air cooling (if used), & on thermal connection of device to a metal chassis or to a heat sink.

→ Typical values for various transistor designs vary from 0.2°C/W for high-power transistor with an efficient heat sink to 1000°C/W for low-power transistor in free air.

→ The max. collector power P_c allowed for safe operation is specified at 25°C

→ For ambient temp.s above this value, P_c must be decreased & at extreme temp at which transistor may operate, P_c is reduced to zero.

→ Condition for Thermal Stability

→ To avoid thermal runaway, the required condition is that the rate at which heat is released at collector junction must not exceed the rate at which the heat can be dissipated

$$\frac{\partial P_c}{\partial T_j} < \frac{\partial P_D}{\partial T_j}$$

→ We have $T_j - T_A = \theta P_D$

Differentiating w.r.t. T_j gives $1 = \theta \frac{\partial P_D}{\partial T_j}$

$$\Rightarrow \frac{\partial P_D}{\partial T_j} = \frac{1}{\theta}$$

$$\therefore \frac{\partial P_c}{\partial T_j} < \frac{1}{\theta}$$

→ This condition must be satisfied to prevent thermal runaway

→ Thermal Stability

→ Consider the self bias ckt and assume that transistor is biased in active region.

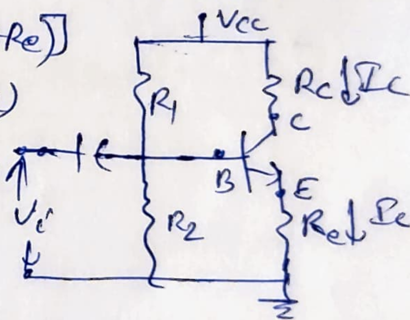
→ The power generated at the collector junction with no signal is

$$P_c = I_c V_{CB} \approx I_c V_{CE}$$

→ If we assume quiescent collector & emitter currents are essentially equal

$$P_c = I_c\left[V_{CC} - I_c(R_c + R_e)\right]$$

$$= I_c V_{CC} - I_c^2 (R_c + R_e)$$



→ The condition to avoid thermal runaway can be rewritten as

$$\frac{\partial P_c}{\partial I_c} \cdot \frac{\partial I_c}{\partial T_j} < \frac{1}{\theta}$$

$$\therefore \frac{\partial P_c}{\partial I_c} = V_{CC} - 2 I_c (R_c + R_e)$$

→ We have $I_c = f(I_{co}, V_{BE}, \beta)$

$$\Delta I_c = \frac{\partial I_c}{\partial I_{co}} \Delta I_{co} + \frac{\partial I_c}{\partial V_{BE}} \Delta V_{BE} + \frac{\partial I_c}{\partial \beta} \Delta \beta$$

$$= S \Delta I_{co} + S' \Delta V_{BE} + S'' \Delta \beta$$

$$\therefore \frac{\partial I_c}{\partial T_j} = S \frac{\partial I_{co}}{\partial T_j} + S' \frac{\partial V_{BE}}{\partial T_j} + S'' \frac{\partial \beta}{\partial T_j}$$

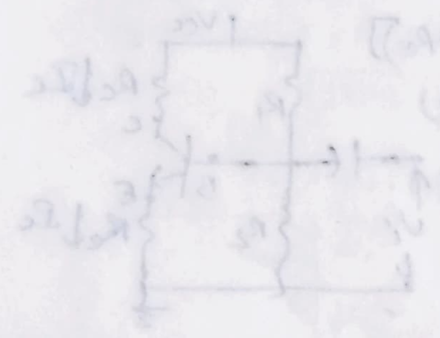
→ In practical the effect of I_{co} dominates for thermal runaway problem, so $\frac{\partial I_c}{\partial T_j} = S \frac{\partial I_{co}}{\partial T_j}$

$$\rightarrow \frac{\partial P_c}{\partial I_c}\left(S \frac{\partial I_{co}}{\partial T_j}\right) < \frac{1}{\theta}$$

→ The reverse saturation current for either silicon or germanium increases about 7%/°C. So $\frac{\partial I_{co}}{\partial T_j} = 0.07 I_{co}$

→ $[V_{cc} - 2I_c(R_e + R_c)](S)(0.07 I_{co}) < \frac{1}{\theta}$

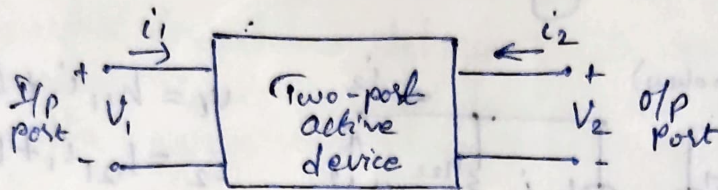
→ This is also valid for p-n-p transistors provided that I_c & I_{co} represent the magnitude of current.



Small Signal Low Frequency BJT Models

→ Two Port Devices and Hybrid Model

→ The terminal behaviour of a large class of two-port devices is specified by two ~~independent~~ voltages & two currents



→ The box represents a two port n/w, so we may select two of four quantities as independent variables & express the remaining two in terms of chosen independent variables.

→ If the current i_1 and the voltage V_2 are independent and if the two-port is linear, then

$$V_1 = h_{11} i_1 + h_{12} V_2$$

$$i_2 = h_{21} i_1 + h_{22} V_2$$

→ The quantities h_{11}, h_{12}, h_{21} & h_{22} are called the h, or hybrid parameters

→ Assuming that there are no reactive elements within two-port n/w, then the h parameters are defined as follows:

$$h_{11} = \left.\frac{V_1}{i_1}\right|_{V_2=0}$$ = i/p resistance with o/p short-ckted (ohms)

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{i_1=0}$$ = fraction of o/p voltage at i/p with i/p open ckted, or reverse-open ckt voltage amplification (dimensionless)

$$h_{21} = \left.\frac{i_2}{i_1}\right|_{V_2=0}$$ = negative of current transfer ratio, or current gain with o/p short-ckted (dimensionless)

$$h_{22} = \left.\frac{i_2}{V_2}\right|_{i_1=0}$$ = o/p conductance with i/p open-ckted (mhos)

→ The following convenient alternative subscript notation is recommended by IEEE standards

$i = 11 =$ i/p $\qquad o = 22 =$ o/p

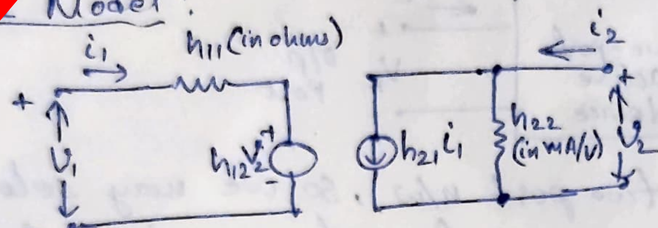
$f = 21 =$ forward transfer $\qquad r = 12 =$ reverse transfer

→ In case of transistors, another subscript (b, e or c) is added to designate the type of configuration.

→ For example $h_{ib} = h_{11b}$ = i/p resistance in common-base configuration, $h_{fe} = h_{21e}$ → short-ckt forward current gain common-emitter ckt

→ If reactive elements are included in the device, the excitation would be considered to be sinusoidal, the h parameters would be functions of freq., & voltage & currents would be represented by phasors V_1, V_2 & I_1, I_2.

Model:



$$v_1 = h_{11}i_1 + h_{12}V_2$$
$$i_2 = h_{21}i_1 + h_{22}V_2$$

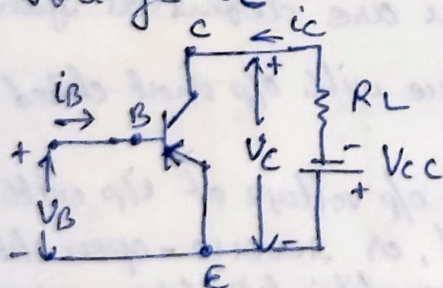
Transistor Hybrid Model

→ The transistor model is given in terms of h parameters, which are real numbers at audio freq's.

→ h-parameters are easy to measure and can be obtained from transistor static characteristics curves and are convenient to use in ckt analysis & design.

→ A set of h-parameters is specified for many transistors by manufacturers.

→ Consider common-emitter connection, the current i_B & voltage V_C are independent variables



$$V_B = f_1(i_B, V_C)$$
$$i_C = f_2(i_B, V_C)$$

→ Making a Taylor's series expansion of above equ's around the quiescent point I_B, V_C & neglecting higher-order terms, we obtain

$$\Delta V_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial f_1}{\partial V_C}\right|_{i_B} \Delta V_C$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{V_C} \Delta i_B + \left.\frac{\partial f_2}{\partial V_C}\right|_{i_B} \Delta V_C$$

→ The quantities ΔV_B, ΔV_C, Δi_B and Δi_C represent the small-signal incremental base & collector voltages & currents can be represented with symbols v_b, v_c, i_b and i_c

$$\therefore \quad V_b = h_{ie} i_b + h_{re} V_c$$

$$i_c = h_{fe} i_b + h_{oe} V_c$$

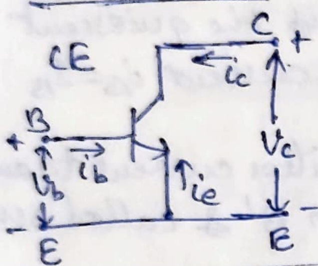
where $h_{ie} = \frac{\partial f_1}{\partial i_B}\Big|_{V_C} = \frac{\partial V_B}{\partial i_B}\Big|_{V_C}$ $\quad h_{re} = \frac{\partial f_1}{\partial V_C}\Big|_{i_B} = \frac{\partial V_B}{\partial V_C}\Big|_{i_B}$

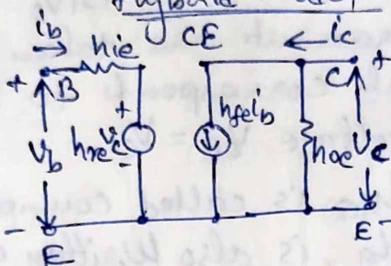
$h_{fe} = \frac{\partial f_2}{\partial i_B}\Big|_{V_C} = \frac{\partial i_C}{\partial i_B}\Big|_{V_C}$ $\quad h_{oe} = \frac{\partial f_2}{\partial V_C}\Big|_{i_B} = \frac{\partial i_C}{\partial V_C}\Big|_{i_B}$

→ The partial derivatives define the h parameters for common-emitter connection. These partial derivatives can be obtained from the transistor characteristic curves & they are real no.s

Three Transistor Configurations

Ckt Schematic | Hybrid model | v-i equations

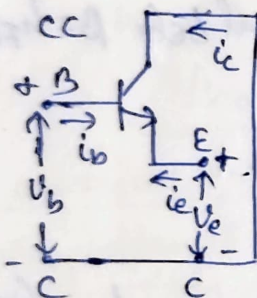


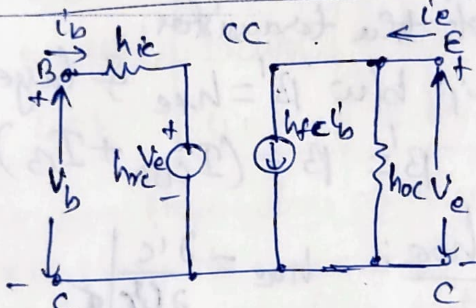


CE

$V_b = h_{ie} i_b + h_{re} V_c$

$i_c = h_{fe} i_b + h_{oe} V_c$

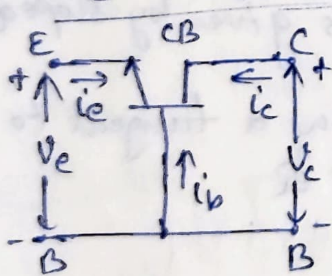


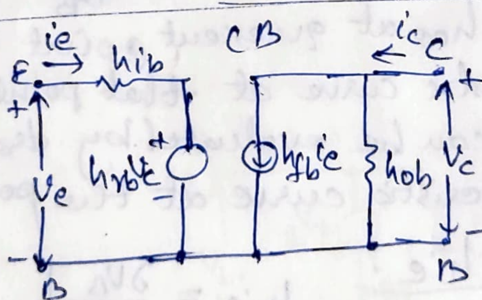


CC

$V_b = h_{ic} i_b + h_{rc} V_e$

$i_e = h_{fc} i_b + h_{oc} V_e$





CB

$V_e = h_{ib} i_e + h_{rb} V_c$

$i_c = h_{fb} i_e + h_{ob} V_c$

→ Above ckts & eqn's are for either an p-n-p or n-p-n transistor & are independent of type of load or method of biasing

→ Determination of h parameters from characteristics

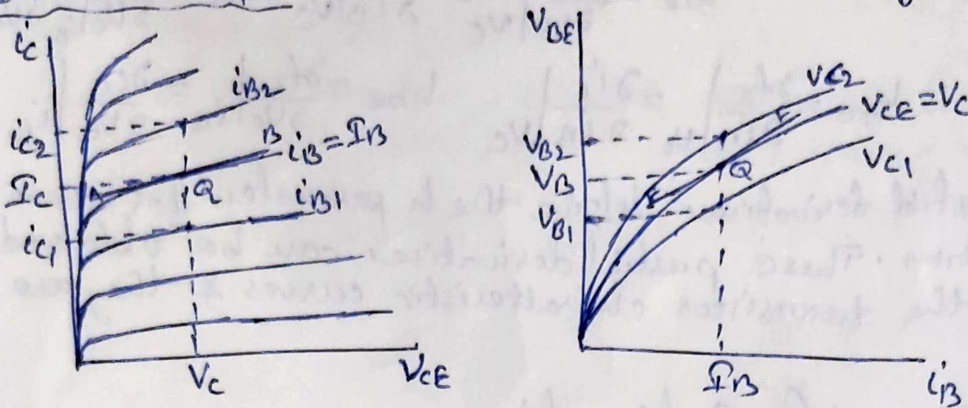
→ Two families of curves are usually specified for transistors

→ The o/p characteristics curves depict the relationship b/w o/p current & voltage, with i/p current as the parameter.

→ The i/p characteristics depict the relationship b/w i/p voltage & current with o/p voltage as the parameter.

→ If i/p & o/p characteristics of a particular connection are given, the h parameters can be determined graphically.

The Parameter h_{fe}: For a common-emitter configuration



From definition $h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{B2} - i_{B1}}$

→ The current increments are taken around the quiescent point Q, which corresponds to base current $i_B = I_B$ & to collector voltage $V_{CE} = V_C$

→ The parameter h_{fe} is called common-emitter current transfer ratio, or CE alpha, is also written α_e or β' & called small signal beta of the transistor.

→ The relationship b/w $\beta' = h_{fe}$ & large-signal beta $\beta = h_{FE}$ is given as $\beta' = \beta + (I_{CBO} + I_B)\frac{\partial \beta}{\partial I_B}$

The Parameter h_{oe}: $h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{I_B}$

→ The value of h_{oe} at quiescent point Q is given by slope of o/p characteristic curve at that point.

→ This slope can be evaluated by drawing a tangent to the characteristic curve at the point Q

The Parameter h_{ie}: $h_{ie} = \left.\frac{\partial V_B}{\partial i_B}\right|_{V_C}$

→ The slope of the appropriate i/p characteristic at Q gives h_{ie}

→ h_{ie} is given by the slope of line which is drawn tangent to characteristic curves at point Q.

The Parameter h_{re}: $h_{re} = \left.\frac{\partial V_B}{\partial V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$

→ The parameter h_{re} can be obtained as change in base voltage, $V_{B2} - V_{B1}$ divided by change in collector voltage, $V_{C1} - V_{C2}$ for a const. base current I_B at Q

→ The procedure for determination of CE h parameters may also be used to obtain the common-base & common-collector h parameters from appropriate i/p & o/p characteristic curves.

Hybrid-Parameter Variations

→ Once a quiescent point Q is specified, h-parameters can be obtained from the slopes & spacing b/w curves at this point.

→ The h-parameters depend upon the position of quiescent point on curves

→ We know that the shape & actual numerical values of characteristics curves depend on junction temperature. Hence the h parameters also depend on temperature.

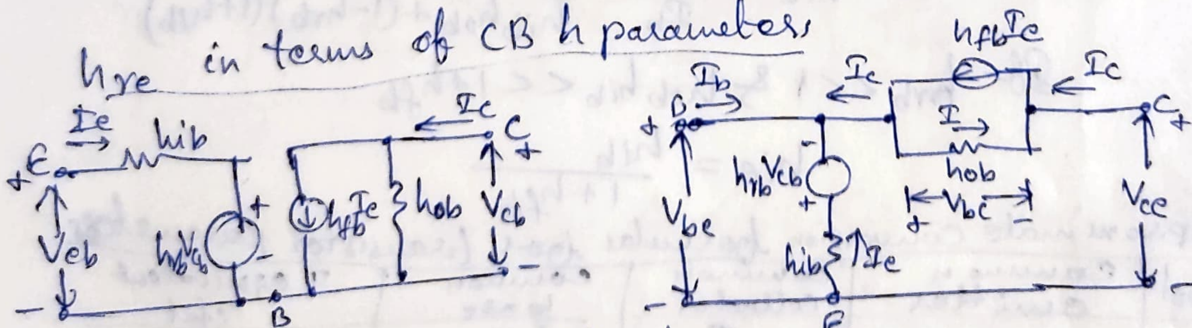
Typical h-parameter values for a transistor (at $I_E = 1.3 mA$)

Parameter	CE	CC	CB
$h_{11} = h_i$	1100 Ω	1100 Ω	21.6 Ω
$h_{12} = h_r$	2.5×10^{-4}	~1	2.9×10^{-4}
$h_{21} = h_f$	50	−51	−0.98
$h_{22} = h_o$	25 μA/V	25 μA/V	0.49 μA/V
$1/h_o$	40K	40K	2.04M

Conversion Formulas for Parameters of Three Transistor Configurations

→ Very often it is necessary to convert from one set of transistor parameters to another set

h_{re} in terms of CB h parameters



$$h_{re} = \frac{V_{be}}{V_{ce}}\bigg|_{I_b=0} = \frac{V_{bc}+V_{ce}}{V_{ce}}\bigg|_{I_b=0} = \left(1 + \frac{V_{bc}}{V_{ce}}\right)\bigg|_{I_b=0}$$

If $I_b = 0$, then $I_c = -I_e$; $\quad I + I_c = h_{fb} I_e$

$\Rightarrow I = (1+h_{fb}) I_e$

$I = h_{ob} V_{bc} = (1+h_{fb}) I_e$ (∵ h_{ob} represents conductance)

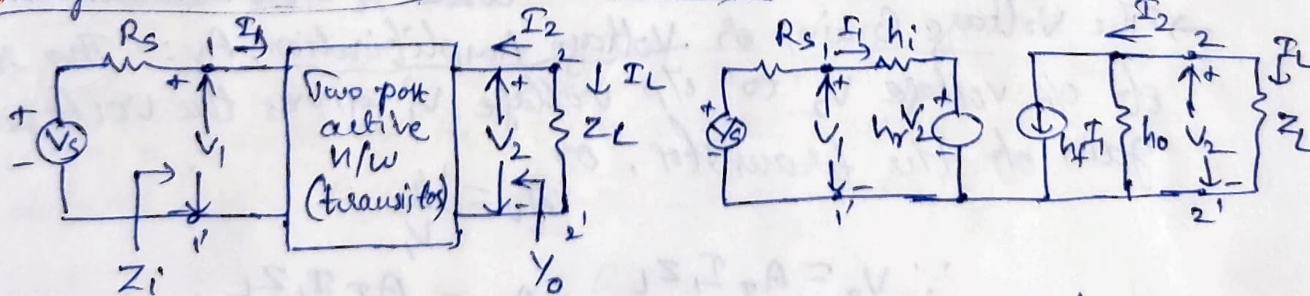
$I_e h_{ib} + h_{rb} V_{cb} + V_{bc} + V_{ce} = 0$

$\Rightarrow \frac{h_{ib} h_{ob} V_{bc}}{1+h_{fb}} - h_{rb} V_{bc} + V_{bc} + V_{ce} = 0$

Symbol	Common emitter	Common collector	Common base	T equivalent circuit
h_{ib}	$\frac{h_{ie}}{1+h_{fe}}$	$-\frac{h_{ic}}{h_{fc}}$	$21.6\,\Omega$	$r_e + (1-a)\,r_b$
h_{rb}	$\frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$	$h_{rc} - \frac{h_{ic}h_{oc}}{h_{fc}} - 1$	2.9×10^{-4}	$\frac{r_e}{r_c}$
h_{fb}	$-\frac{h_{fe}}{1+h_{fe}}$	$-\frac{1+h_{fc}}{h_{fc}}$	-0.98	$-a$
h_{ob}	$\frac{h_{oe}}{1+h_{fe}}$	$-\frac{h_{oc}}{h_{fc}}$	$0.49\,\mu A/V$	$\frac{1}{r_c}$
h_{ic}	h_{ie} *	$1100\,\Omega$	$\frac{h_{ib}}{1+h_{fb}}$	$r_b + \frac{r_e}{1-a}$
h_{rc}	$1-h_{re} \approx 1$ *	1	1	$1 - \frac{r_e}{(1-a)r_c}$
h_{fc}	$-(1+h_{fe})$ *	-51	$-\frac{1}{1+h_{fb}}$	$-\frac{1}{1-a}$
h_{oc}	h_{oe} *	$25\,\mu A/V$	$\frac{h_{ob}}{1+h_{fb}}$	$\frac{1}{(1-a)r_c}$
a	$\frac{h_{fe}}{1+h_{fe}}$	$\frac{1+h_{fc}}{h_{fc}}$	$-h_{fb}$	0.980
r_c	$\frac{1+h_{fe}}{h_{oe}}$ *	$-\frac{h_{fc}}{h_{oc}}$ *	$\frac{1}{h_{ob}}$	$2.04\,M\Omega$
r_e	$\frac{h_{re}}{h_{oe}}$ *	$-\frac{1-h_{rc}}{h_{oc}}$ *	$h_{ib} - \frac{h_{rb}(1+h_{fb})}{h_{ob}}$ *	$10\,\Omega$
r_b	$h_{ie} - \frac{h_{re}}{h_{oe}}(1+h_{fe})$ *	$h_{ic} + \frac{h_{fc}(1-h_{rc})}{h_{oc}}$ *	$\frac{h_{rb}}{h_{ob}}$ *	$590\,\Omega$

* exact

Analysis of a Transistor Amplifier Circuit using h-parameters



→ To form a transistor amplifier it is only necessary to connect an external load & signal source & to bias the transistor properly.

→ Considering transistor in any one of 3 possible configuration and replacing the transistor with its small-signal hybrid-model.

~~→ The current gain or current amplification, A_I for the~~

→ Assuming sinusoidally varying voltages & currents, we can proceed with the analysis of the ckt using the phasor (sinor) notation to represent the sinusoidally varying quantities.

→ **The current gain or current amplification A_I**:- for the transistor amplifier stage, A_I is defined as the ratio of o/p to i/p currents, or

$$A_I = \frac{I_L}{I_1} = -\frac{I_2}{I_1}$$

From o/p ckt $I_2 = h_f I_1 + h_o V_2$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$ in I_2

$$I_2 = h_f I_1 - h_o I_2 Z_L \Rightarrow I_2(1 + h_o Z_L) = h_f I_1$$

$$\therefore A_I = -\frac{I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}$$

→ **The Input Impedance Z_i**:- The impedance we see looking into amplifier i/p terminals (1-1') is the amplifier i/p impedance Z_i, or

$$Z_i = \frac{V_1}{I_1}$$

From i/p ckt, $V_1 = h_i I_1 + h_r V_2$

$$Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1} = h_i + h_r \frac{V_2}{I_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$ in V_2 of Z_i

$$\therefore Z_i = h_i + h_r \frac{A_I I_1 Z_L}{I_1}$$

$$Z_i = h_i + h_r A_I Z_L = h_i - \frac{h_f h_r}{Y_L + h_o}$$

Note:- I/p impedance is a function of load impedance

where Y_L = load admittance $= 1/Z_L$

→ **The Voltage Gain, or Voltage Amplification, A_V**:- The ratio of o/p voltage V_2 to i/p voltage V_1 gives the voltage gain of the transistor, or

$$A_V = \frac{V_2}{V_1}$$

$\because V_2 = A_I I_1 Z_L$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = A_I \frac{Z_L}{Z_i}$$

The Output Admittance Y_o:- For the transistor Y_o is defined as $Y_o \equiv \frac{I_2}{V_2}$ with $V_s = 0$

$\because I_2 = h_f I_1 + h_o V_2$, $Y_o = \frac{h_f I_1 + h_o V_2}{V_2} = h_f \frac{I_1}{V_2} + h_o$

With $V_s = 0$ for i/p ckt $R_s I_1 + h_i I_1 + h_r V_2 = 0$

$$\Rightarrow \frac{I_1}{V_2} = -\frac{h_r}{h_i + R_s}$$

So $Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$

Note:- O/p admittance is function of the source resistance

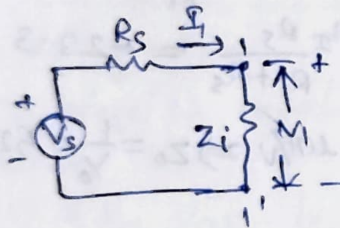
→ If source impedance is resistive (R_s), then Y_o is real (a conductance)

→ From definition $Y_o = \frac{1}{Z_o}$

→ **The Voltage Amplification A_{Vs}, Taking into Account the Resistance R_s of Source:-**

→ The overall voltage voltage gain A_{Vs} is defined by

$$A_{Vs} \equiv \frac{V_2}{V_s} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_s} = A_V \frac{V_1}{V_s}$$



From the equivalent i/p ckt of amplifier

$$V_1 = V_s \frac{Z_i}{Z_i + R_s}$$

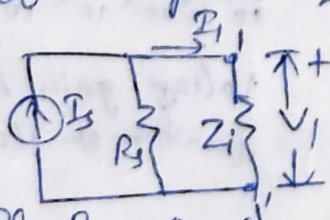
Then $A_{Vs} = A_V \frac{Z_i}{Z_i + R_s} = \frac{A_I Z_L}{Z_i + R_s}$ $\left(\because A_V = A_I \frac{Z_L}{Z_i}\right)$

If $R_s = 0$, then $A_{Vs} = A_V$, so A_V is the voltage gain for an ideal voltage source (one with zero external resistance)

If Z_i is resistive & equal in magnitude to R_s then $A_{Vs} = 0.5 A_V$

The Current Amplification A_{Is}, Taking into Account the Source Resistance R_s:-

→ If the i/p source is a current generator I_s in parallel with a resistance R_s, then overall current gain is defined by $A_{Is} \equiv -\frac{I_2}{I_s} = -\frac{I_2}{I_1} \frac{I_1}{I_s} = A_I \cdot \frac{I_1}{I_s}$



$$I_1 = I_s \frac{R_s}{R_s + Z_i}$$

$$\therefore A_{Is} = \frac{A_I R_s}{R_s + Z_i}$$

→ If $R_s = \infty$ then $A_{Is} = A_I$, so A_I is current gain for an ideal current source (one with infinite source resistance)

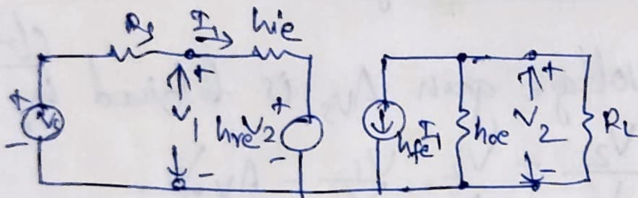
→ The voltage & current gains, taking source impedance into account, are related by
$$A_{Vs} = A_{Is} \frac{Z_L}{R_s}$$

→ The Operating Power Gain A_p :- The average power delivered to the load Z_L is $P_2 = |V_2||I_L| \cos\theta$, where θ is phase angle b/w V_2 & I_L

→ Assuming Z_L is resistive, $P_2 = V_2 I_L = -V_2 I_2$

→ Since the i/p power is $P_1 = V_1 I_1$, the operating power gain A_p of transistor is defined as
$$A_p = \frac{P_2}{P_1} = -\frac{V_2 I_2}{V_1 I_1} = A_V A_I = A_I^2 \frac{R_L}{R_i}$$

Q. A transistor is connected as a common-emitter amplifier, & the h-parameters are $h_{ie} = 1100\Omega$, $h_{re} = 2.5 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25\mu A/V$. If $R_L = R_s = 1000\Omega$ find the gains and i/p & o/p impedances.



$$A_I = \frac{-h_{fe}}{1 + h_{oe}R_L} = -48.8$$

$$R_i = h_{ie} + h_{re} A_I R_L = 1088\Omega$$

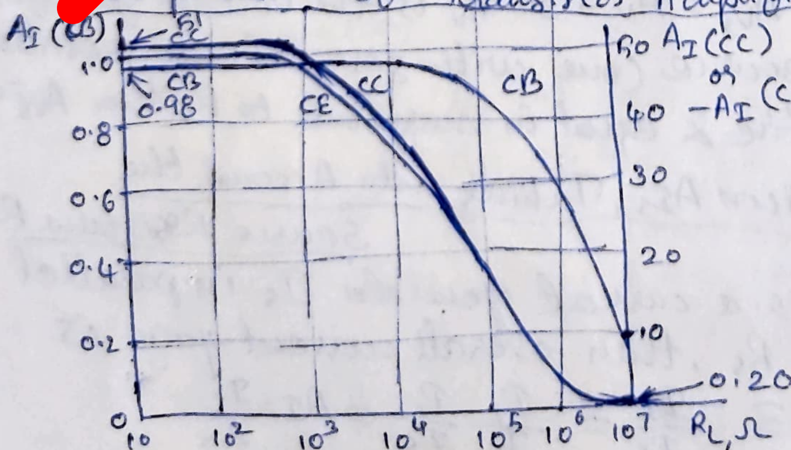
$$A_V = A_I \frac{R_L}{R_i} = -44.8$$

$$A_{Vs} = \frac{A_V R_i}{R_i + R_s} = -23.3, \quad A_{Is} = \frac{A_I R_s}{R_i + R_s} = -23.3$$

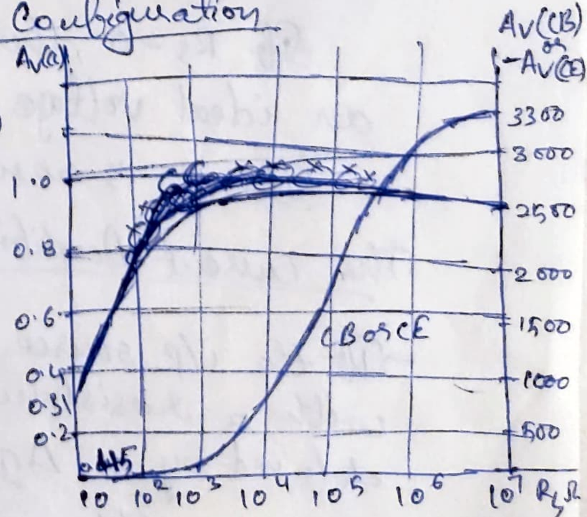
$$Y_o = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s} = 19 \times 10^{-6} \mho = 19\, \mu A/V \Rightarrow Z_o = \frac{1}{Y_o} = 52.6 k\Omega$$

$$A_p = A_V A_I = 2190$$

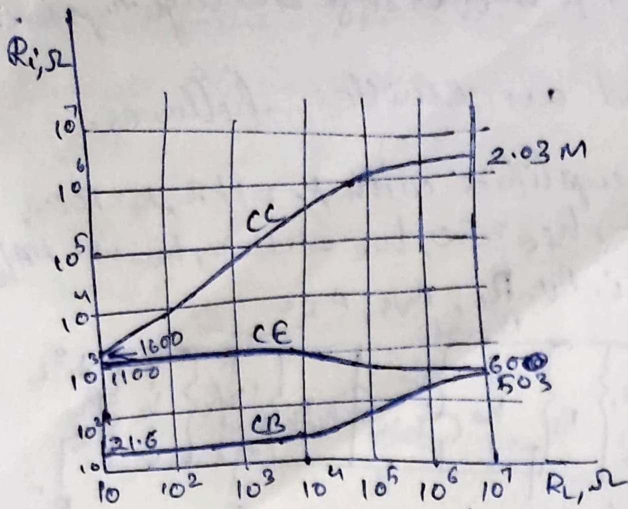
→ Comparision of Transistor Amplifier Configuration



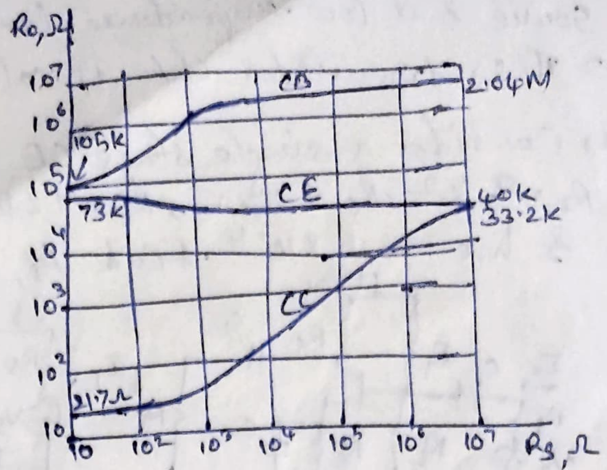
Current gain A_I as a function of its load resistance



Voltage gain A_V as a function of its Load resistance



I/p resistance as a function of its load resistance



~~CE Configuration~~ Comparison of transistor configurations

Quantity	CE	CC	CB
A_I	High (−46.5)	High (47.5)	Low (0.98)
A_V	High (−131)	Low (0.99)	High (131)
R_i (R_L = 3kΩ)	Medium (1065Ω)	High (144 KΩ)	Low (22.5Ω)
R_o (R_S = 3kΩ)	Medium high (45.5kΩ)	Low (80.5Ω)	High (1.72MΩ)

CE configuration

→ CE stage is capable of both a voltage gain & a current gain greater than unity.

→ R_i & R_o vary least with R_L & R_s respectively for CE ckt.

→ R_i & R_o lie b/w those for CB & CC configurations.

→ This is most versatile & useful of 3 connections

CB Configuration

→ For CB stage, A_I is less than unity

→ A_V is high (approx.ly equal to that of CE stage)

→ R_i is lowest & R_o is highest of 3 configurations

→ CB stage has few applications.

→ It is used to match a very low impedance source, to drive a high impedance load, or as a non-inverting amplifier with a voltage gain greater than unity.

→ It is also used as a const. current source.

CC configuration

→ For CC stage, A_I is high (approx.ly equal to that of CE stage)

A_V is less than unity

R_i is highest & R_o is lowest of 3 configurations

Different Coupling Schemes used in Amplifiers

→ When amplifiers are cascaded, it is necessary to use a coupling n/w b/w the o/p of one amplifier & the i/p of the following amplifier. This type of coupling is called inter stage coupling.

→ These coupling n/ws serve the following 2 purposes:

1) It transfers the a.c. o/p of one stage to i/p of the next stage
2) It isolates the d.c. conditions of one stage to the next.

→ Three coupling schemes commonly used in multi-stage amplifiers are:

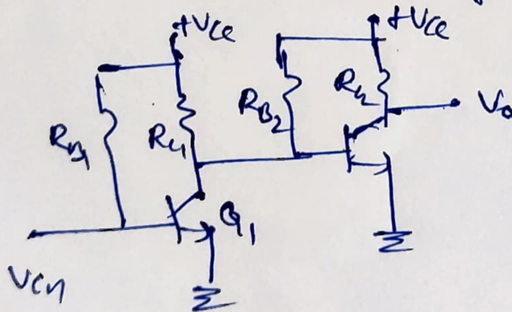
1) Resistance-Capacitance (RC) Coupling
2) Transformer coupling
3) Direct coupling.

Direct coupling :- In this method, the a.c o/p signal is fed directly to the next stage. No reactance is included in the coupling ckt.

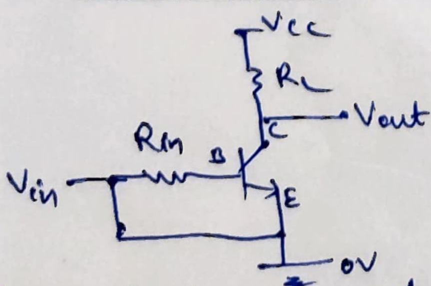
→ Special d.c. voltage level ckts are used to match the o/p d.c. levels.

→ It is used when amplification of low freq. signals is to be done.

→ Amplifiers using this coupling schemes are called direct-coupled amplifiers or d.c. amplifiers



Transistor as a Switch



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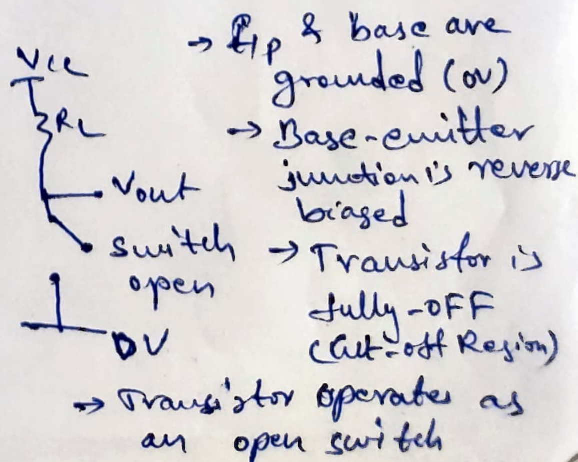


→ I/p & base are grounded (0V)

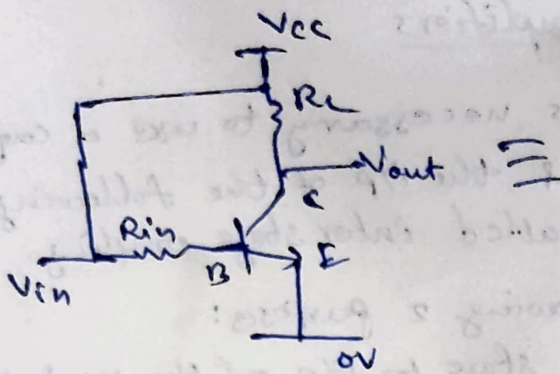
→ Base-emitter junction is reverse biased

→ Transistor is fully-OFF (Cut-off Region)

→ No collector current ($I_c = 0$)

→ $V_{out} = V_{CE} = V_{CC} = $ "1"

→ Transistor operates as an open switch



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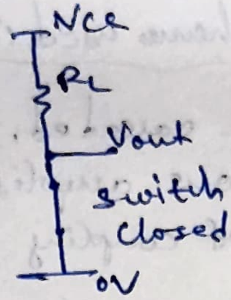


→ I/p & base are connected to Vcc

→ Base-emitter junction is forward biased

→ Transistor is fully ON (Saturation Region)

→ Max. collector current flows $\left(I_C = \frac{V_{CC}}{R_L}\right)$

→ $V_{CE} = 0$ (Ideal saturation)

→ $V_{out} = V_{CE} =$ "0"

→ Transistor operates as a closed switch.

Problems

Q. In a certain transistor, 99.6% of carriers injected into base cross the collector-base junction. If leakage current is 5μA & the collector current is 20 mA, calculate i) the value of α_{dc}
ii) the emitter current.

$I_C = 0.996 I_E$, $I_{CBO} = 5\mu A$, $I_C = 20$ mA

$\alpha = \frac{I_C}{I_E} = 0.996$

$I_C = \alpha I_E + I_{CBO} \Rightarrow I_E = \frac{I_C - I_{CBO}}{\alpha} = 20.07$mA

Q. Calculate the values of collector current & base current for a transistor with $\alpha = 0.99$ & $I_{CBO} = 10\mu A$. The emitter current is measured as 8 mA

$\alpha = 0.99$, $I_{CBO} = 10\mu A$, $I_E = 8$ mA

$I_C = \alpha I_E + I_{CBO} = 7.93$mA

$I_B = I_E - I_C = (1-\alpha) I_E - I_{CBO} = 70\mu A$

Q. If $\beta = 100$, $I_{CBO} = 10\mu A$ & $I_B = 80\mu A$, find I_E

$I_C = \beta I_B + (1+\beta) I_{CBO}$

$I_E = I_B + I_C = (1+\beta) I_B + (1+\beta) I_{CBO}$

$= 9.09$mA

Q. If $\alpha = 0.98$, $I_{CBO} = 10\mu A$ & $I_B = 100\mu A$, find I_E

$I_E = (1+\beta) I_B + (1+\beta) I_{CBO}$

$\beta = \frac{\alpha}{1-\alpha} = 49$

$I_E = 5.5$mA

Q. If the base current in a transistor is 20μA when the emitter current is 6.4mA, what are the values of α and β? Also calculate the collector current.

$I_B = 20\mu A$, $I_E = 6.4$mA,

$I_C = I_E - I_B = 6.38$mA

$\beta = \frac{I_C}{I_B} = 319$

$\alpha = \frac{\beta}{\beta + 1} = 0.9968$

Q. The reverse leakage current of transistor, when connected in common-base configuration is 0.1 μA, while it is 16 μA when the same transistor is connected in common emitter configuration. Calculate α & β of transistor.

$I_{CBO} = 0.1\,\mu A \quad I_{CEO} = 16\,\mu A$

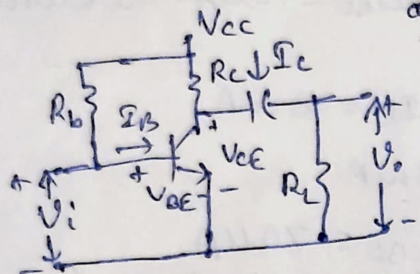
$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO} \Rightarrow 1-\alpha = \frac{I_{CBO}}{I_{CEO}} \Rightarrow \alpha = 1 - \frac{I_{CBO}}{I_{CEO}}$$

$$\therefore \alpha = 0.993$$

$$\beta = \frac{\alpha}{1-\alpha} = 159$$

Q. Consider a fixed bias ckt where an n-p-n silicon transistor with $\beta = 90$ is used with $V_{CC} = 15V$, $R_C = 3K\Omega$, $R_b = 1M\Omega$. Assume $V_{BE} = 0.6V$. (a) Find the quiescent point (or Q-point) of ckt & (b) Obtain the equation for ac Load line for $R_L = 1K\Omega$

a) $V_{CC} = 15V$, $R_C = 3K\Omega$, $V_{BE} = 0.6V$, $R_b = 1M\Omega$, $\beta = 90$



$$I_B = \frac{V_{CC} - V_{BE}}{R_b} = 14.4\,\mu A$$

$$I_C = \beta I_B = 1.296\,mA$$

$$V_{CE} = V_{CC} - I_C R_C = 12.408V$$

Thus the operating point, quiescent point, or Q-point is $I_C = 1.296\,mA$ & $V_{CE} = 12.41V$ on dc load line (which cuts V_{CE} at $V_{CC} = 15V$ & I_C at $\frac{V_{CC}}{R_C} = 7.5mA$)

b) Under ac condition $R_L' = \frac{R_C R_L}{R_C + R_L} = \frac{2}{3}K\Omega$ $(R_L = 1K\Omega)$

Since ac load line must pass through Q point ($I_C = 1.296mA$, $V_{CE} = 12.41V$) & has a slope of $-\frac{1}{R_L'}$

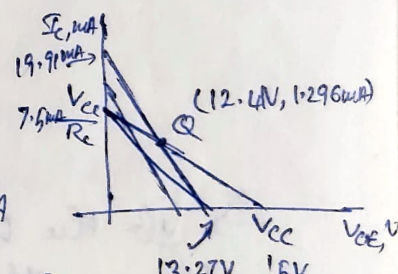
$$I_C - (1.296mA) = -\frac{V_{CE} - (12.41V)}{(2/3\,K\Omega)}$$

Putting $I_C = 0 \Rightarrow V_{CE} = 13.27V$

Thus ac load line cuts V_{CE} at $13.27V$

Putting $V_{CE} = 0 \Rightarrow I_C = 19.91\,mA$

So ac load line cuts I_C at $19.91mA$

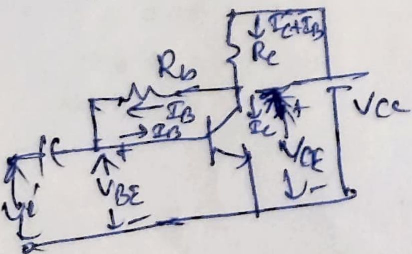


Q. The silicon type transistor is biased in collector-to base bias with $\beta = 50$, $V_{CC} = 10V$ & $R_C = 250\Omega$. Find R_b & calculate S. Operating point is chosen at $I_B = 0.4mA$, $I_C = 21mA$, $V_{CE} = 4.6V$ [$V_{CE} = V_{CC} - I_C R_C$ (neglecting I_B)]

$$R_b = \frac{V_{CE} - V_{BE}}{I_B}$$

$\beta = 50$, $V_{CC} = 10V$, $R_C = 250\Omega$

$$= 10K\Omega$$



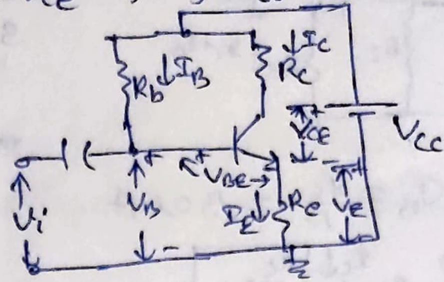
$$S = \frac{1+\beta}{1 + \frac{\beta R_C}{R_C + R_b}} = 23$$

Q. A transistor with $\beta = 100$ is to be used in emitter feedback bias configuration. The collector ckt resistance is $R_C = 1.5K\Omega$, the emitter ckt resistance $R_E = 2K\Omega$ & $V_{CC} = 12V$. Assume $V_{BE} = 0.6V$

$I_{co} = 0$. (a) Find R_b ...
$V_{CE} = 5V$, (b) Find the stability factor S.

(a) $R_c = 1.5k\Omega$, $R_e = 2k\Omega$, $V_{cc} = 12V$, $V_{ce} = 5V$ & $I_{co} = 0$

$$I_c = \frac{V_{cc} - V_{CE}}{R_c + R_e}$$
$$= 2\,mA$$



$$I_c = \frac{\beta\left[(V_{cc} - V_{BE}) + (R_e + R_b) I_{co}\right]}{\beta R_e + R_b}$$

$$\beta R_e + R_b = \frac{\beta\left[V_{cc} - V_{BE}\right]}{I_c} \quad (\because I_{co} = 0)$$

$$\Rightarrow R_b = \beta\left[\frac{(V_{cc} - V_{BE})}{I_c} - R_e\right] = 370k\Omega$$

(b)
$$S = \frac{1+\beta}{1 + \beta \frac{R_e}{R_e + R_b}} = 65$$

Q. A transistor with $\beta = 100$ is used in collector-emitter feedback bias configuration. Assume $R_C = 1.5k\Omega$, $R_e = 2k\Omega$, $R_b = 370k\Omega$, $V_{cc} = 12V$, $V_{BE} = 0.6V$ & $I_{co} = 0$. (a) Calculate the collector-to-emitter voltage V_{CE} & (b) find the stability factor S

(a) $R_c = 1.5k\Omega$, $R_e = 2k\Omega$, $R_b = 370k\Omega$, $V_{cc} = 12V$, $V_{BE} = 0.6V$ & $I_{co} = 0$, $\beta = 100$

$$I_c = \frac{\beta\left[(V_{cc} - V_{BE}) + (R_e + R_c + R_b) I_{co}\right]}{\beta(R_e + R_c) + R_b}$$

$$= \frac{\beta(V_{cc} - V_{BE})}{\beta(R_e + R_c) + R_b} = 1.58\,mA$$

$$I_c = \beta I_B + (1+\beta) I_{co}$$

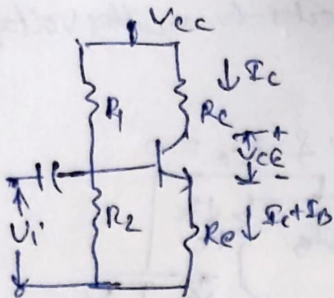
Since $I_{co} = 0$, $I_c = \beta I_B \Rightarrow I_B = \frac{I_c}{\beta} = 15.8\,\mu A$

$$V_{CE} = V_{cc} - (I_c + I_B)(R_c + R_e) = 6.41V$$

(b)
$$S = \frac{1+\beta}{1 + \frac{\beta(R_c + R_e)}{R_c + R_e + R_b}} = 52.14$$

Q. Assume that a silicon transistor with $\beta = 50$, $V_{BE} = 0.6V$, $V_{cc} = 22.5V$ & $R_c = 5.6k\Omega$ is used in self bias. Q point is $V_{CE} = 12V$, $I_C = 1.5mA$ & a stability factor $S \leq 3$. Find R_e, R_1 & R_2

$\beta = 50$, $V_{BE} = 0.6V$, $V_{CC} = 22.5V$, $R_c = 5.6k\Omega$, $V_{CE} = 12V$, $I_C = 1.5mA$
$S = 3$



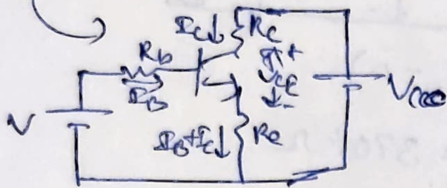
$$R_e + R_c = \frac{V_{CC} - V_{CE}}{I_C} = 7.0\,k\Omega$$

$$\Rightarrow R_e = 1.4\,k\Omega$$

$$S = \frac{1+\beta}{1+\beta\frac{R_e}{R_e+R_b}} = \frac{(1+\beta)(1+R_b/R_e)}{1+\beta+R_b/R_e} = 3$$

$$\Rightarrow \frac{R_b}{R_e} = 2.12 \Rightarrow R_b = 2.96\,k\Omega$$

$$I_B = \frac{I_C}{\beta} = 30\,\mu A$$



$$V = \frac{V_{CC} R_2}{R_1+R_2} \Rightarrow R_1 = \frac{R_b V_{CC}}{V}\,;\; R_2 = \frac{R_1 V}{V_{CC}-V}$$

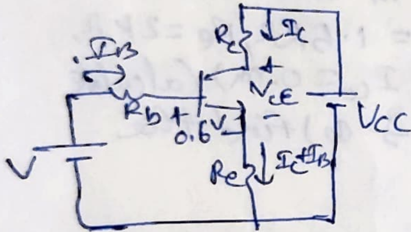
$$V = I_B R_b + V_{BE} + (I_B + I_C) R_e$$

$$= 2.83\,V$$

$$R_1 = \frac{R_b V_{CC}}{V} = 23.6\,k\Omega$$

$$R_2 = \frac{R_1 V}{V_{CC}-V} = 3.38\,k\Omega$$

Q: A silicon transistor whose ~~common emitter~~ is used in self bias with $V_{CC} = 22.5\,V$, $R_C = 5.6\,k\Omega$, $R_e = 1\,k\Omega$, $R_2 = 10\,k\Omega$ & $R_1 = 90\,k\Omega$. For this transistor $\beta = 55$. (a) Find Q point (b) Calculate S



$$V = \frac{V_{CC} R_2}{R_1+R_2} = 2.25\,V \quad R_b = \frac{R_1 R_2}{R_1+R_2} = 9\,k\Omega$$

$$-V_{CC} + I_C R_C + (I_B + I_C) R_e + V_{CE} = 0$$

$$\Rightarrow -22.5 + 6.6 I_C + I_B + V_{CE} = 0 \quad (1)$$

$$-V + I_B R_b + V_{BE} + (I_C + I_B) R_e = 0 \quad (2)$$

$$\Rightarrow -2.25 + 0.6 + 10 I_B + I_C = 0$$

$$I_C = \beta I_B$$

$$\text{so } -1.65 + I_C + \frac{10}{55} I_C = 0$$

$$\Rightarrow I_C = 1.40\,mA$$

$$\& \; I_B = \frac{I_C}{55} = 25.5\,\mu A$$

From (1) & (2)

~~$V_{CE} = 65 I_B + 11.6$~~

$$-22.5 + 6.6 I_C + I_B + V_{CE} = 0$$

$$\Rightarrow V_{CE} = 13.2\,V$$

(b) $$S = \frac{(1+\beta)(1+R_b/R_e)}{1+\beta+R_b/R_e} = 8.61$$

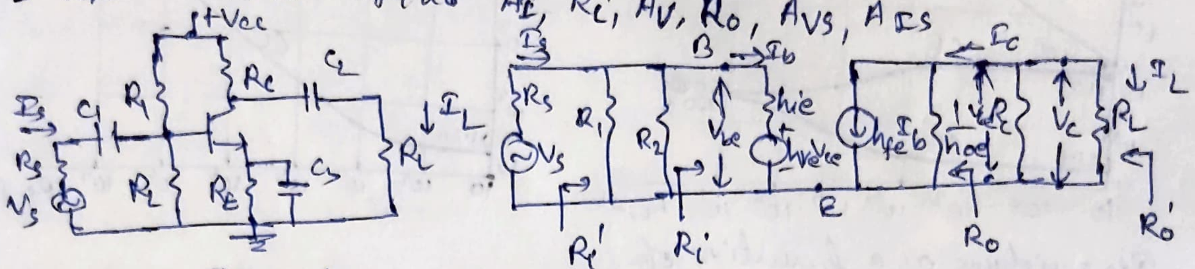
→ Find the value of θ required for the transistor used in self bias configuration in order for the ckt to be thermally stable. Assume $I_{CO} = 1\,nA$ at $25\,°C$. $V_{CC} = 22.5$, $I_C = 1.4\,mA$, $R_e = 1\,k\Omega$, $R_c = 5.6\,k\Omega$, $S = 8.61$.

$$[V_{CC} - 2 I_C (R_e + R_c)](S)(0.07 I_{CO}) < \frac{1}{\theta}$$

$$2.42 \times 10^{-9} < \frac{1}{\theta} \Rightarrow \theta < 4.1 \times 10^{8}\,°C/W$$

→ This ckt finds wide application as a buffer stage b/w high-impedance source & a low-impedance load.
→ This transistor ckt is called an emitter follower.

Q. Consider a single stage CE amplifier with $R_S = 1k\Omega$, $R_1 = 50k\Omega$, $R_2 = 2k\Omega$, $R_C = 1k\Omega$, $R_L = 1.2k\Omega$, $h_{fe} = 50$, $h_{ie} = 1.1k\Omega$, $h_{oe} = 25\,\mu A/V$ & $h_{re} = 2.5\times10^{-4}$. Find A_I, R_i, A_V, R_o, A_{VS}, A_{IS}



Current gain, $A_I = \frac{-I_L}{I_b} = \frac{-h_{fe}}{1+h_{oe}R_L'}$ where $R_L' = R_C \| R_L = 545.45\Omega$

$= -49.32$

I/p resistance, $R_i = h_{ie} + h_{re} A_I R_L' = 1093\Omega$

voltage gain, $A_V = \frac{V_{ce}}{V_{be}} = A_I \frac{R_L'}{R_i} = -24.61$

O/p resistance, $R_o = \frac{1}{h_{oe} - \frac{h_{fe}h_{re}}{R_S' + h_{ie}}}$ where $R_S' = R_S \| R_1 \| R_2$

Overall I/p resistance, $R_i' = R_i \| R_1 \| R_2 = 4.933k\Omega$

Overall o/p resistance, $R_o' = R_o \| R_C \| R_L$

Overall voltage gain, $A_{VS} = \frac{V_{ce}}{V_S} = A_V \frac{R_i'}{R_S + R_i'} = 10.1$

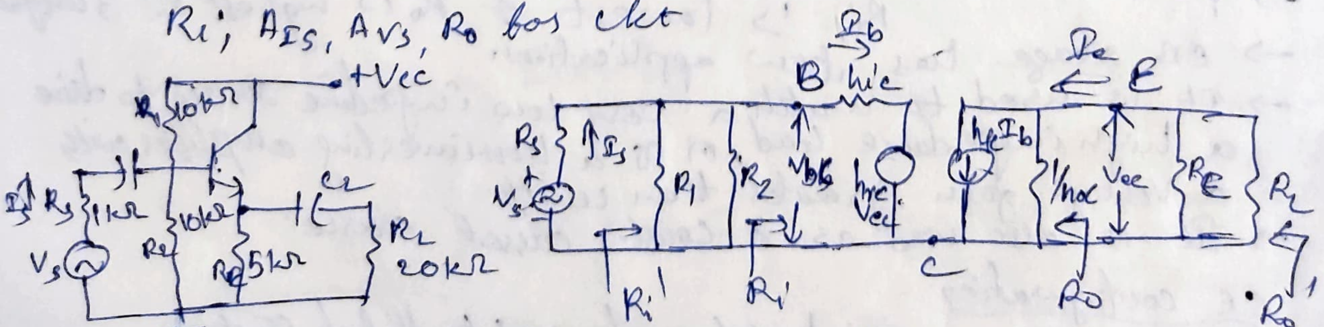
$\frac{V_{ce}}{V_S} = \frac{V_{ce}}{V_{be}} \times \frac{V_{be}}{V_S}$

Overall current gain, $A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_C} \times \frac{I_C}{I_b} \times \frac{I_b}{I_S} = \frac{R_C}{R_C + R_L} \times (A_I) \times \frac{R_B}{R_B + R_i}$

$= -14.29$

$R_B = R_1 \| R_2$

Q. In common collector amplifier, the transistor parameters are $h_{ic} = 1.2k\Omega$, $h_{fc} = -101$ & $h_{oc} = 25\,\mu A/V$. Calculate R_i, A_{IS}, A_{VS}, R_o for ckt



current Gain, $A_I = \frac{I_e}{I_b} = \frac{-h_{fc}}{1+h_{oc}R_L'}$ where $R_L' = R_E \| R_L$

$= 91.81$

I/p Resistance, $R_i = h_{ic} + h_{rc} A_I R_L' = 368.44 k\Omega$

Overall I/p Resistance, $R_i' = R_i || R_1 || R_2 = 4.933 k\Omega$

Voltage Gain, $A_V = A_I \frac{R_L'}{R_i'} = 0.996$

Overall Voltage Gain, $A_{VS} = A_V \frac{R_i'}{R_i' + R_S}$

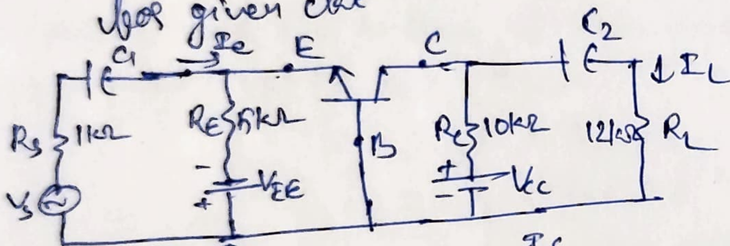
Overall current Gain, $A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_e} \times \frac{I_e}{I_b} \times \frac{I_b}{I_S} = \frac{-R_E}{R_E + R_L} \times (A_I) \times \frac{R_B}{R_B + R_i}$
$= 0.246$

O/p Resistance, $R_O = \frac{1}{h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_S'}}$ where $R_S' = R_S || R_1 || R_2$
$= 833.33 \Omega$

$= 20.12 \Omega$

Overall O/p Resistance, $R_O' = R_O || R_L' = 20 \Omega$

Q For common base ckt, the transistor parameters are $h_{ib} = 22 \Omega$, $h_{fb} = -0.98$, $h_{ob} = 0.49 \mu A/V$, $h_{rb} = 2.9 \times 10^{-4}$. Calculate the values of i/p resistance, o/p resistance, current gain & voltage gain for given ckt.



Current gain, $A_I = \frac{-h_{fb}}{1 + h_{ob} R_L'}$

where $R_L' = R_C || R_L$
$= 5.45 k\Omega$

$A_I = -0.977$

I/p resistance, $R_i = h_{ib} + h_{rb} A_I R_L'$
$= 20.45 \Omega$

Overall I/p resistance, $R_i' = R_i || R_E$
$= 20.36 \Omega$

voltage gain, $A_V = \frac{A_I R_L'}{R_i} = -260$

Overall Voltage gain, $A_{VS} = A_V \cdot \frac{R_i'}{R_i' + R_S} = -5.18$

Overall current gain $A_{IS} = \frac{I_L}{I_S} = \frac{I_L}{I_C} \times \frac{I_C}{I_e} \times \frac{I_e}{I_S}$
$= \frac{-R_C}{R_C + R_L} \times (-A_I) \times \frac{R_E}{R_E + R_i} = 0.442$

O/p Resistance, $R_O = \frac{1}{h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_S'}}$ where $R_S' = R_S || R_E = 833.33 \Omega$
$= 1.21 M\Omega$

Overall O/p Resistance, $R_O' = R_O || R_L' = 5.425 k\Omega$

UNIT - II

BIPOLAR JUNCTION TRANSISTOR, TRANSISTOR BIASING AND STABILIZATION

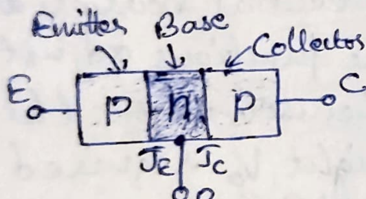
The Junction Transistor

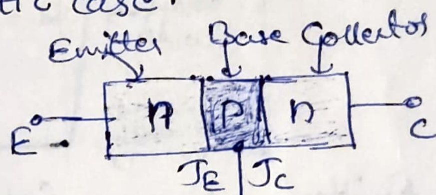
→ A junction transistor consists of a silicon (or germanium) crystal in which a layer of n-type silicon is sandwiched b/w two layers of p-type silicon.

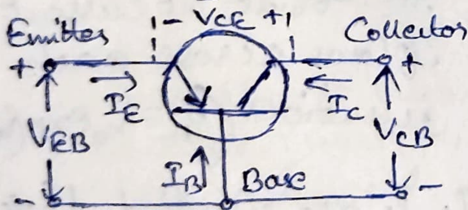
→ Alternatively, a transistor may consist of p-type b/w two layers of n-type material.

→ In the former case the transistor is referred to as a p-n-p transistor, & in the later case, as an n-p-n transistor.

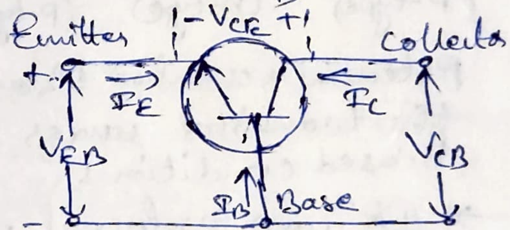
→ The semiconductor sandwich is extremely small and is hermetically sealed againt moisture inside a metal or plastic case.







p-n-p type



n-p-n type

Circuit representation of p-n-p & n-p-n transistors

→ The 3 portions of a transistor are known as emitter, base, and collector.

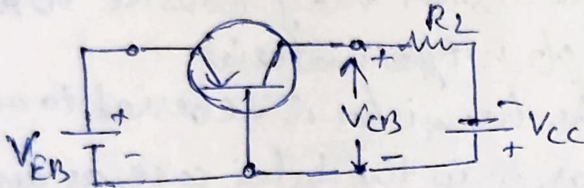
→ The arrow of the emitter lead specifies the direction of current flow when the emitter-base junction is biased in forward direction.

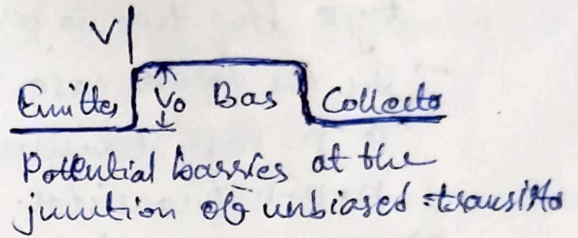
→ In both cases, the emitter, base, and collector currents are I_E, I_B and I_C respectively, are assumed positive when the currents flow into the transistor.

→ The symbols V_{EB}, V_{CB} & V_{CE} are the emitter-base, collector-base, and collector-emitter voltages, respectively.

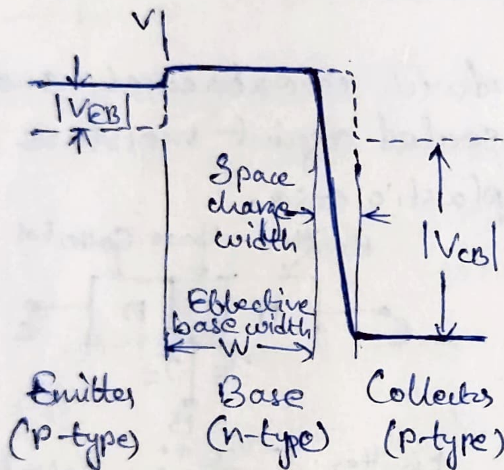
→ <u>Potential Distribution through a Transistor</u>

↳ Consider a p-n-p transistor with voltage sources which serve to bias the emitter-base junction in the forward direction & the collector-base junction in the reverse direction.





Potential barriers at the junction of unbiased transistor



Emitter (p-type) Base (n-type) Collector (p-type)

Potential variation through the transistor under biased conditions.

→ In the absence of applied voltage, the potential barriers at the junctions adjust themselves to the height V_0 required so that no current flows across each junction. $\left(P_{P0} = P_{n0} \exp(V_0/V_T)\right)$

→ If now external potentials are applied, these voltages appear essentially across the junctions.

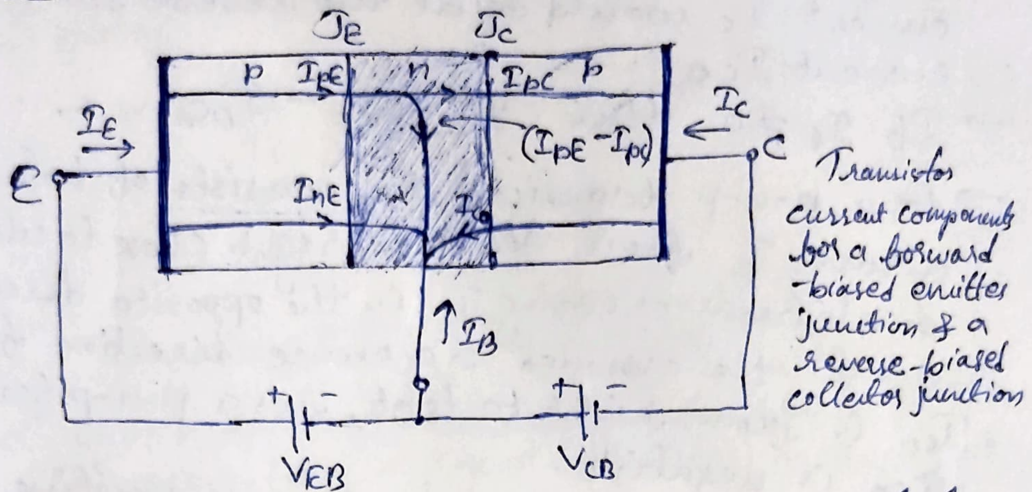
→ Hence forward biasing of emitter-base junction lowers the emitter-base potential barrier by $|V_{EB}|$, whereas reverse biasing of the collector-base junction increases the collector-base potential barrier by $|V_{CB}|$.

→ The lowering of emitter-base barrier permits the emitter current to increase, & holes are injected into the base region.

→ The potential is const. across the base region, & the injected holes diffuse across the n-type material to the collector-base junction.

→ The holes which reach this junction fall down the potential barrier, & are therefore collected by collector.

Transistor Current Components



Transistor current components for a forward-biased emitter junction & a reverse-biased collector junction

→ The emitter current components I_E consists of hole current I_{pE} (holes crossing from emitter into base) and electron current I_{nE} (electrons crossing from base into the emitter).

→ The ratio of hole to electron currents I_{pE}/I_{nE}, crossing the emitter junction is proportional to the ratio of the conductivity of p-material to that of n-material.

→ In a commercial transistor the doping of emitter is made much larger than the doping of the base.

→ This feature ensures (in a p-n-p transistor) that the emitter current consists almost entirely of holes, since the current which results from electrons crossing the emitter junction from base to emitter does not contribute carriers which can reach the collector.

→ Not all the holes crossing the emitter junction J_E reach the collector junction J_C because some of them combine with the electrons in the n-type base.

→ If I_{pC} is the hole current at J_C, there must be a bulk recombination current $I_{pE}-I_{pC}$ leaving the base (actually, electrons enter the base region through the base lead to supply those charges which have been lost by recombination with the holes injected into the base across J_E)

→ If the emitter were open-ckted so that $I_E = 0$, then I_{pC} would be zero.

→ Under these circumstances, the base & collector would acts as a reverse-biased diode; & the collector current I_C would equal the reverse saturation current I_{CO}.

→ If $I_E \neq 0$, then $I_C = I_{CO} - I_{pC}$

→ For a p-n-p transistor I_{CO} consists of holes moving across J_C from left to right (base to collector) & electrons crossing J_C in the opposite direction.

→ Since the assumed reference direction for I_{CO} is from right to left, for a p-n-p transistor, I_{CO} is negative.

→ For an n-p-n transistor I_{CO} is positive.

→ Emitter Efficiency γ

↳ The emitter or injection efficiency γ is defined as

$$\gamma = \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}}$$

→ In the case of p-n-p transistor,

$$\gamma = \frac{I_{pE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_E}$$

where I_{pE} is injected hole diffusion current at emitter junction & I_{nE} is injected electron diffusion current at emitter junction.

→ Transport Factor β^*

↳ The transport factor β^* is defined as

$$\beta^* = \frac{\text{injected carrier current reaching } J_C}{\text{injected carrier current at } J_E}$$

→ In case of p-n-p transistor,

$$\beta^* = \frac{I_{pC}}{I_{pE}}$$

→ Large Signal Current Gain α

↳ The ratio of the -ve of the collector-current increment to the emitter-current change from zero (cutoff) to I_E as the large-signal current gain of a common-base transistor.

$$\alpha \equiv -\frac{I_C - I_{CO}}{I_E}$$

→ since I_C & I_E have opposite signs, α is always +ve.

→ Typical numerical values of α lie in the range of 0.90 to 0.995.

$$\alpha = \frac{I_{pC}}{I_E} \quad (\because I_C = I_{CO} - I_{pC})$$

$$= \frac{I_{pC}}{I_{pE}} \cdot \frac{I_{pE}}{I_E}$$

$$\therefore \alpha = \beta^* \gamma \quad \left(\beta^* = \frac{I_{pC}}{I_{pE}} \;\&\; \gamma = \frac{I_{pE}}{I_E}\right)$$

→ α^* is the ratio of total current crossing J_C to the hole current (for a p-n-p transistor) arriving at the junction.

→ For most transistors, $\alpha^* = 1$

→ α is not a const., but varies with emitter current I_E, collector voltage V_{CB}, & temperature.

→ If the transistor is in active region (i.e. if emitter is forward-biased & collector is reverse-biased), the collector current is given by ——①

$$I_C = -\alpha I_E + I_{CO}$$

→ In active region the collector current is essentially independent of collector voltage & depends only upon the emitter current.

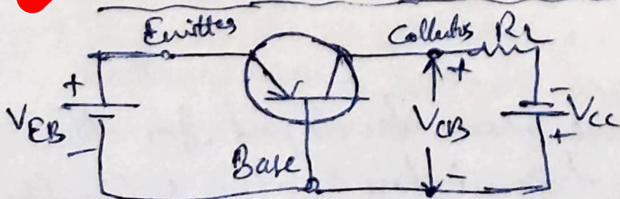
→ To generalize the above equation ①, we need to replace I_{CO} by the current in a p-n diode (that consisting of base & collector regions).

→ $$I_C = -\alpha I_E + I_{CO}\left(1 - \exp(V_C/V_T)\right) \quad —②$$

where the symbol V_C represents the drop across J_C from the p to the n side

→ If V_C is negative & has a magnitude large compared with V_T then ② reduces to ①

The Transistor as an Amplifier



→ A small-voltage change ΔV_i b/w emitter & base causes a relatively large emitter-current change ΔI_E.

→ We define a symbol α' that is fraction of this current change which is collected & passes through R_L

→ The change in o/p voltage across the load resistor $\Delta V_o = \alpha' R_L \Delta I_E$ may be many times the change in i/p voltage ΔV_i

→ Under these conditions, the voltage amplification $A = V_o / \Delta V_i$ will be greater than unity, & transistor acts as an amplifier.

→ If the dynamic resistance of emitter junction is r_e' then $\Delta V_i = r_e' \Delta I_E$ &

$$A = \frac{\alpha' R_L \Delta I_E}{r_e' \Delta I_E} = \frac{\alpha' R_L}{r_e'}$$

→ $r_e' = \frac{26}{I_E}$ $\left(\because r = \frac{\eta V_T}{I} = \frac{26}{I} \text{ for } \eta = 1 \text{ at room temperature, I in mA}\right)$

where I_E is quiescent emitter current in mAs

→ If $r_e' = 40\Omega$, $\alpha' = -1$ & $R_L = 3000\Omega$, then $A = -75$

→ It is clear that current in the low-resistance i/p ckt is transferred to high-resistance o/p ckt.

→ The word "transistor" which originated as a contraction of "transfer resistor" is based upon the above physical picture of the device.

→ The transistor provides power gain as well as voltage or current amplification.

→ <u>The Parameter α'</u>

↳ α' is defined as the ratio of change in collector current to change in emitter current at const. collector-to base voltage & is called the small-signal forward short-circuit current transfer ratio or gain

→ Specifically $\alpha' = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_B}$ on the assumption that α is independent of I_E

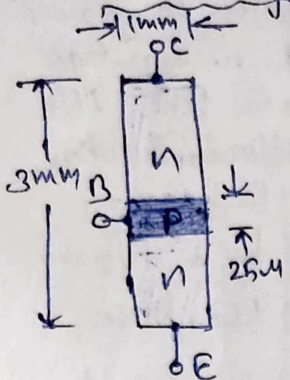
→ From ①, $\alpha' = -\alpha$

<u>Transistor Construction</u>

→ Five basic techniques have been developed for the manufacture of diodes, transistors & other semiconductor devices.

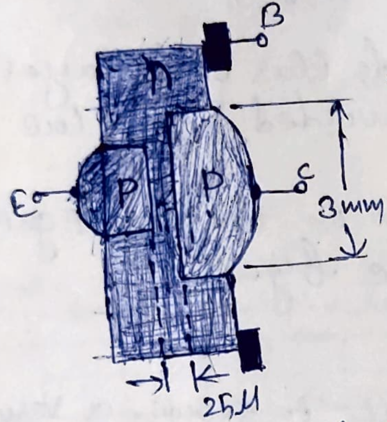
→ They are: grown, alloy, electro-chemical, diffusion, or epitaxial

↳ Grown Type



→ It is made by drawing a single crystal from a melt of silicon or germanium whose impurity concentration is changed during the crystal-drawing operation by adding n- or p-type atoms as required.

↳ Alloy Type



→ This technique, also called the fused construction.

→ The center (base) section is a thin wafer of n-type material

→ Two small dots of indium are attached to opposite sides of wafer.

→ The whole structure is raised for a short time to a high temperature, above the melting point of indium but below that of germanium.

→ The indium dissolves the germanium beneath it & forms a saturation solution.

→ On cooling, the germanium in contact with the base material recrystallizes with enough indium concentration to change it from n type to p type.

→ The collector is made larger than the emitter, so that the collector subtends a large angle as viewed from the emitter.

→ Because of this geometrical arrangement, very little emitter current follows a diffusion path which carries it to the base rather than to the collector.

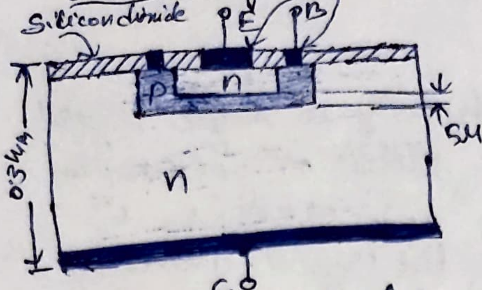
↳ Electrochemically Etched Type

→ This technique consists in etching depressions on opposite sides of a semiconductor wafer in order to reduce the thickness of the base section.

→ The emitter & collector junctions are then formed by electroplating a suitable metal into the depression areas

→ This type of device, also referred to as a surface-barrier transistor, is no longer of commercial importance

↳ **Diffusion Type**



→ This technique consists in subjecting a semiconductor wafer to gaseous diffusions of both n- & p-type impurities to form both the emitter & the collector junctions.

→ In this process, the base-collector junction area is determined by a diffusion mask which is photoetched just prior to the base diffusion.

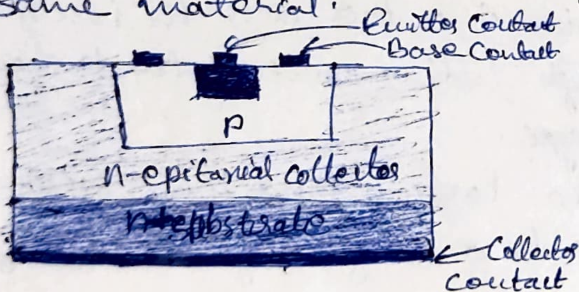
→ The emitter is then diffused on the base, & a final layer of silicon dioxide is thermally grown over the entire surface.

→ Because of passivating action of this oxide layer, most surface problems are avoided & very low leakage currents result.

→ There is also an improvement in the current gain at low currents & in the noise figure.

↳ **Epitaxial Type**

→ The epitaxial technique consists in growing a very thin, high-purity, single crystal layer of silicon or germanium on a heavily doped substrate of same material.



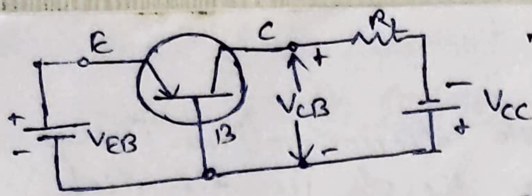
→ This augmented crystal forms the collector on which the base & emitter may be diffused.

Common-Base Configuration

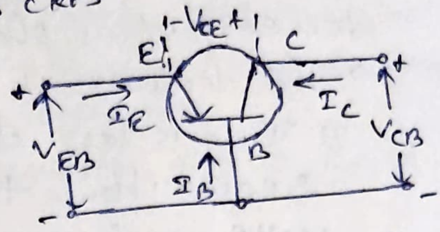
→ Many different families of characteristic curves can be ~~uniquely~~ drawn depending upon which two parameters are chosen as independent variables.

→ In the case of the transistor, it turns out to be most useful to select the i/p current & o/p voltage as the independent variables.

→ The o/p current & i/p voltage are expressed graphically in terms of the independent variables.



→ This shows a p-n-p transistor in a grounded-base configuration
→ This ckt is referred to as a common base, or CB configuration, since the base is common to the i/p & o/p ckts.



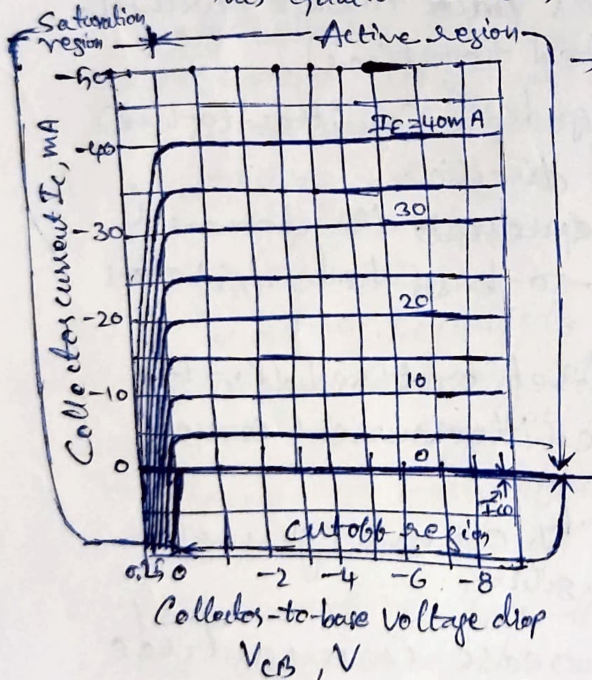
→ We may completely describe the transistor of common base configuration by the following 2 relations, which give the i/p voltage V_{EB} & o/p current I_C in terms of the o/p voltage V_{CB} & i/p current I_E:

$$V_{EB} = \phi_1(V_{CB}, I_E) \quad \text{— (1)}$$

$$I_C = \phi_2(V_{CB}, I_E) \quad \text{— (2)}$$

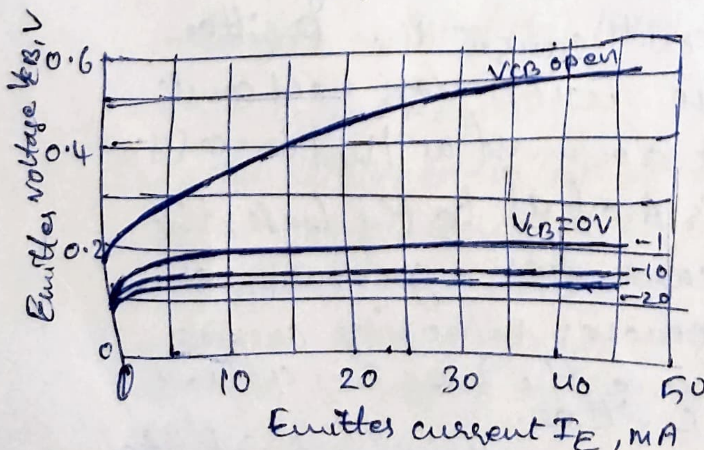
↓

This equation is read, "I_C is some function ϕ_2 of V_{CB} & I_E"



→ This is a plot of collector current I_C versus collector-to-base voltage drop V_{CB}, with emitter current I_E as a parameter for a typical p-n-p germanium transistor represents the relation $I_C = \phi_2(V_{CB}, I_E)$

→ These curves are known as the o/p or collector static characteristics.



→ This is a plot of emitter-to-base voltage V_{EB} versus emitter current I_E, with collector-to-base voltage V_{EB} as a parameter for a typical p-n-p germanium transistor represents the relation $V_{EB} = \phi_1(V_{CB}, I_E)$

→ This set of curves is referred to as i/p or emitter static characteristics.

The Early Effect

↳ An increase in magnitude of collector voltage increases the space-charge width at the o/p junction diode. Such action causes the effective base width W to decrease, this phenomenon is known as Early Effect

→ This decrease in W has 2 consequences:

1) There is less chance for recombination within the base region. Hence the transport factor β^* & also α increase with an increase in magnitude of collector junction voltage.
2) The charge gradient is increased within the base & consequently, the current of minority carriers injected across the emitter junction increases.

The Input Characteristics

↳ It is easy to understanding the i/p & o/p characteristics if we consider that transistor consists of two diodes placed in series "back to back" (with the two cathodes connected together) . . .

→ In active region the i/p diode (emitter-to-base) is biased in forward direction.

→ The i/p characteristics represents the forward characteristic of emitter-to-base diode for various collector voltages.

→ There exists a cutin, offset, or threshold voltage V_γ, below which the emitter current is very small.

→ In general, V_γ is approx. 0.1 V for germanium transistors & 0.5 V for silicon.

→ By Early effect, an increase in magnitude of collector voltage will cause the emitter current to increase, with V_{EB} held const.

→ Thus the curves shift downward as $|V_{CB}|$ increases.

→ When the collector is shorted to the base, the emitter current increases for a given V_{EB} since the collector now removes minority carriers from the base, & hence the base can attract more holes from emitter.

→ This means that the curve with $V_{CB}=0$ is shifted downward from the collector characteristic marked "V_{CB} open"

The Output Characteristics

↳ The collector-to-base diode is normally biased in reverse direction

→ For $I_E = 0$, the collector current $I_C = I_{CO}$

→ For other values of I_E, the o/p-diode reverse current is augmented by the fraction of the i/p-diode forward current which reaches the collector.

→ I_{CO} is -ve for a p-n-p transistor & +ve for a n-p-n transistor.

Active Region

↳ In this region the collector junction is biased in the reverse direction & the emitter junction in the forward direction.

→ Consider first that the emitter current is zero. Then the collector current is small & equals the reverse saturation current I_{CO} (μAs for Ge & nAs for Si) of collector junction considered as a diode.

→ Suppose now that a forward emitter current I_E is caused to flow in the emitter ckt. Then a fraction $-\alpha I_E$ of this current will reach the collector, ~~voltage~~ & I_C is therefore given by

$I_C = -\alpha I_E$.

→ In active region, the collector current is essentially independent of collector voltage & depends only upon the emitter current.

→ Because of Early effect, there is a small (perhaps 0.5%) increase in $|I_C|$ with $|V_{CB}|$

→ Because α is less than, but almost equal to unity, the magnitude of collector current ~~with small changes~~ is (slightly) less than that of emitter current

Saturation Region

↳ The region to the left of the ordinate $V_{CB} = 0$, & above $I_E = 0$ characteristics in which both emitter & collector junctions are forward-biased, is called saturation region.

→ For a forward bias, I_C increases exponentially with voltage according to the diode relationship $\{I_C = a_{21}[\exp(V_E/V_T) - 1] + a_{22}[\exp(V_C/V_T) - 1]\}$

→ A forward bias means that the collector p material is made +ve w.r.t. base n side, & hence the hole current flows from p-side to n-material.

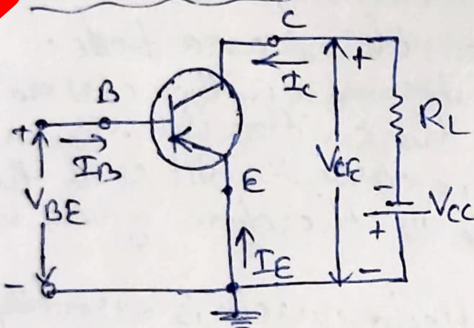
→ The hole flow corresponds to a +ve change in collector current. Hence the collector current increases rapidly.

→ I_C may even become +ve if the forward bias is sufficiently large.

→ Cutoff Region

↳ The region below & to the right of $I_E = 0$ characteristic, for which the emitter & collector junctions are both reverse-biased, is referred to as cutoff region.

The Common-Emitter Configuration



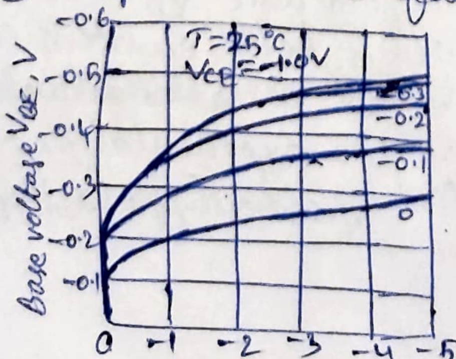
→ Most transistor ckts have the emitter, rather than base, as the terminal common to both i/p & o/p.

→ In common-emitter configuration, the i/p current & o/p voltage are taken as independent variables, whereas the i/p voltage & o/p current are the dependent variables

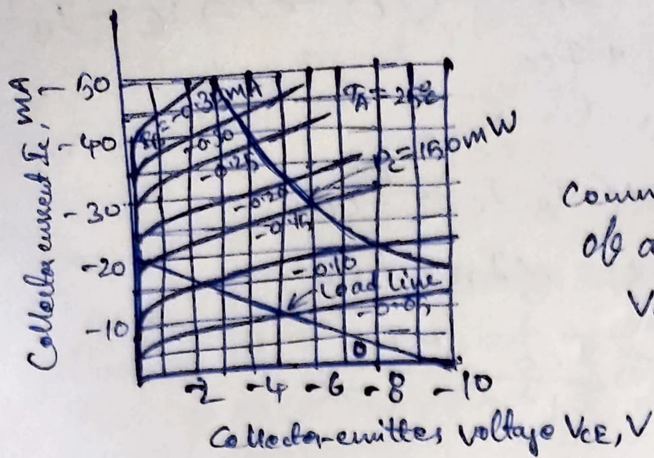
$$V_{BE} = f_1(V_{CE}, I_B) \quad \text{—} (1)$$

$$I_C = f_2(V_{CE}, I_B) \quad \text{—} (2)$$

→ (1) represents the family of i/p characteristic curves
(2) represents the family of o/p characteristic curves



Common-emitter i/p characteristics of p-n-p germanium transistor



Common-emitter o/p characteristics of a p-n-p germanium transistor
$V_{CC} = 10V$, $R_L = 500\Omega$

→ **The Input Characteristics**

→ The abscissa is the base current I_B, the ordinate is the base-to-emitter voltage V_{BE}, & the curves are drawn for various values of collector-to-emitter voltage, V_{CE}.

→ In general, increasing $|V_{CE}|$ with const. V_{BE} causes a decrease in base width W (the Early Effect) & results in a decreasing recombination base current.

→ The i/p characteristics for silicon are similar to that of germanium. The only notable difference in the case of silicon is that curves break away from zero current in the range 0.5 to 0.6 V, rather than in range 0.1 to 0.2 V as for germanium.

→ **The Output Characteristics**

→ This family of curves may be divided into three regions - the active region, the cut off and the saturation regions

→ In active region, the collector junction is reverse-biased & the emitter junction is forward biased.

→ The active region is the area to the right of the ordinate V_{CE} = a few tenths of a volt & above $I_B = 0$

→ In this region the transistor o/p current responds most sensitively to an i/p signal. So if the transistor is to be used as an amplifying device without appreciable distortion, it must be restricted to operate in this region

→ The base current is $I_B = -(I_C + I_E) \Rightarrow I_E = -I_B - I_C$

→ We have $I_C = -\alpha I_E + I_{CO}$ ....

→ Combining these equations

$$I_C = -\alpha(-I_B - I_C) + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$\Rightarrow I_C = \frac{I_{CO}}{1-\alpha} + \frac{\alpha I_B}{1-\alpha} \ldots$$

CE Cutoff Region

→ We have $I_C = -\alpha I_E + I_{CO}$

→ From CE configuration, if $I_B = 0$, then $I_E = -I_C$

$$\therefore I_C = -I_E = \frac{I_{CO}}{1-\alpha} \equiv I_{CEO}$$

→ The actual collector current with collector junction reverse biased & base open-ckted is designated by the symbol I_{CEO}

→ Even in the neighbourhood of cutoff, α may be as large as 0.9 for germanium, then $I_C \simeq 10 I_{CO}$ at zero base current.

→ So in order to cut off the transistor it is not enough to reduce I_B to zero. Instead, it is necessary to reverse-bias the emitter junction slightly.

→ We shall define cutoff as the condition where the collector current is equal to the reverse saturation current I_{CO} & the emitter current is zero.

→ In silicon, at collector currents of the order of I_{CO} it is found that α is very nearly zero because of recombination in the emitter junction transition region.

→ Hence even with $I_B = 0$, we find that $I_C = I_{CO} = -I_E$ so that the transistor is still very close to cutoff.

→ In silicon, cutoff occurs at $V_{BE} \simeq 0V$, corresponding to a base short-ckted to the emitter

→ In summary, cutoff means that $I_E = 0$, $I_C = I_{CO}$, $I_B = -I_C = -I_{CO}$ & V_{BE} is a reverse voltage whose magnitude is of order of 0.1 V for germanium & 0V for a silicon transistor

Reverse Collector Saturation Current I_{CBO}

→ The collector current in a physical transistor (a real, nonidealized, or commercial device) when the emitter current is zero is designated by the symbol I_{CBO}

→ Two factors cooperate to make $|I_{CBO}|$ larger than $|I_{CO}|$.

1) There exists a leakage current which flows, not through the junction, but around it & across the surfaces. The leakage current is proportional to the voltage across junction.

2) New carriers may be generated by the collision in the collector junction transistion region, leading to avalanche multiplication of current & eventual breakdown.

→ At 25°c, I_{CBO} for a Ge transistor whose power dissipation is in the range of some hundreds of milliwatts is of the order of μAs & for a Si transistor I_{CBO} is the range of nAs

→ The temperature sensitivity of I_{CBO} in silicon is approx. ly same as that of germanium

→ It is found that the temp. coefficient of I_{CBO} is 8%/°C for Ge & 6%/°C

→ Using 7% as an average value & since $(1.07)^{10} \simeq 2$ we see that I_{CBO} approx. ly doubles for every 10°C increase in temperature for both Ge & Si.

→ Because of lower absolute value of I_{CBO} in silicon, these transistors may be used up to about 200°C, where Ge transistors are limited to about 100°C.

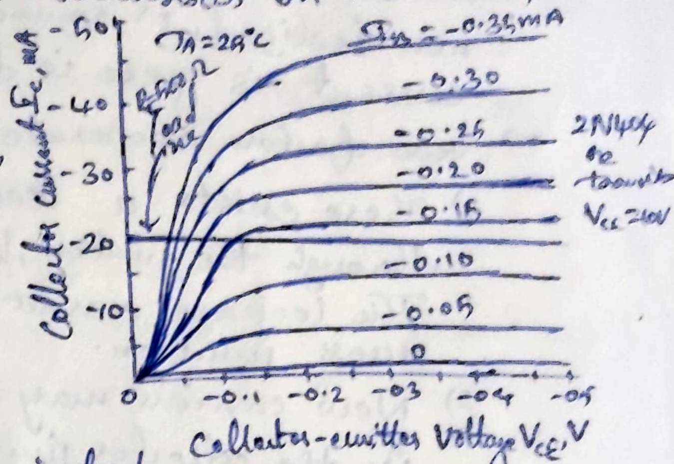
The CE Saturation Region

→ The saturation region may be defined as the one where the collector junction (as well as emitter junction) is forward-biased.

→ In this region bottoming occurs, $|V_{CE}|$ drops to a few tenths of a volt, & collector current is approx. ly independent of base current, for given values of V_{CC} & R_L

→ In saturation, the collector current is nominally V_{CC}/R_L, & since R_L is small, it may be necessary to

Keep V_{CC} correspondingly small in order to stay within the limitations imposed by the transistor on maximum current & dissipation.



__Saturation Resistance:-__ For a transistor operating in the saturation region, a quantity of interest is the ratio $V_{CE(sat)}/I_C$.

→ This parameter is called the common-emitter saturation resistance, variously abbreviated R_{CS}, R_{CES}, or $R_{CE(sat)}$.

→ To specify R_{CS} properly, we must indicate the operating point at which it was determined.

__Saturation Voltages:-__ Manufacturers may specify R_{CS} for several values of I_B or they may supply curves of $V_{CE(sat)}$ & $V_{BE(sat)}$ as functions of I_B & I_C.

→ The saturation voltage $V_{CE(sat)}$ depends not only on operating point, but also on semiconductor material (Ge or Si) & on the type of transistor construction.

→ Ge transistors have lower values for $V_{CE(sat)}$ than Si

→ Alloy junction & epitaxial transistors give the lowest values for $V_{CE(sat)}$ (corresponding to about 1 Ω saturation resistance), whereas grown-junction transistors yield the highest

→ Typical values of the temp. coefficient of saturation voltages are ~ −2.5 mV/°C for $V_{BE(sat)}$ & approx.ly one-tenth of this value for $V_{CE(sat)}$ for either Ge or Si.

__The dc Current Gain h_{FE}:-__ A transistor parameter of interest is the ratio I_C/I_B, where I_C is collector current & I_B is the base current

→ The quantity is designated by β_{dc} or h_{FE}, & is known as dc beta, the dc forward current transfer ratio, or dc current gain.

→ In the saturation region, the parameter h_{FE} is a useful number & one which is usually supplied by the manufacturer when a switching transistor is involved.

→ Commercially available transistors have values of h_{FE} that cover the range from 10 to 150 at collector currents as small as 5 mA & as large as 30 A

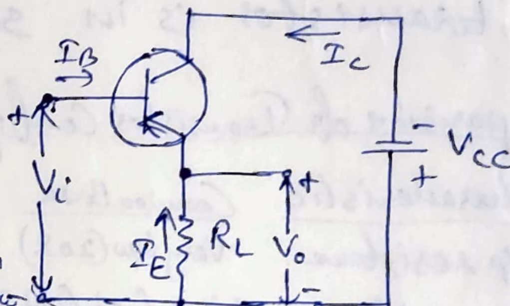
Tests for Saturation:-

1) If I_C & I_B can be determined independently from the ckt under consideration, the transistor is in saturation if $|I_B| \geq |I_C|/h_{FE}$.

2) If V_{CB} is determined from the ckt. configuration & if this quantity is +ve for a p-n-p transistor (or -ve for an n-p-n), transistor is in saturation.

The Common-Collector Configuration

→ The ckt is basically the same as the CE configuration except that the load resistor is in emitter ckt rather than in collector ckt.



→ If we specify the operation for that common-collector ckt in terms of currents which is flow, the operation for the much the same as for the common emitter configuration

→ When base current is I_{CO}, the emitter current will be zero & no current will flow in the load.

→ ~~When base current~~ As the transistor is brought out of this back-biased condition by increasing the magnitude of the base current, the transistor will pass through the active region & eventually reach saturation.

→ In this condition all the supply voltage, except for a very small drop across the transistor, will appear across the load.

Large-Signal, dc & Small-signal CE Values of Current Gain

→ We define $\beta = \frac{\alpha}{1-\alpha}$

& Replacing I_{CO} by I_{CBO} in $I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CO}}{1-\alpha}$

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$\Rightarrow \quad \beta = \frac{I_C - I_{CBO}}{I_B - (-I_{CBO})}$$

→ In CE cutoff region we define cutoff to mean that $I_E = 0$, $I_C = I_{CBO}$ & $I_B = -I_{CBO}$

→ Consequently β gives the ratio of collector-current increment to the base current change from cutoff to I_B

→ Hence β represents the large-signal current gain of a common-emitter transistor.

→ In CE saturation region, we define the dc current gain by $\beta_{dc} \equiv \frac{I_C}{I_B} \equiv h_{FE}$

→ h_{FE} is most useful in determining whether or not a transistor is in saturation.

Comparision of Transistor Configurations

Characteristic	Common Base	Common Emitter	Common Collector
I/p resistance	Very low (20Ω)	Low (1KΩ)	High (500KΩ)
O/p resistance	Very high (1MΩ)	High (40KΩ)	Low (50Ω)
I/p current	I_E	I_B	I_B
O/p current	I_C	I_C	I_E
I/p voltage applied b/w	Emitter & Base	Base & Emitter	Base & Collector
O/p voltage applied b/w	Collector & Base	Collector & Emitter	Emitter & Collector
Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B}$
Current gain	Less than unity	High (20 to few hundred)	High (20 to few hundred)
Voltage gain	Medium	Medium	Low
Applications	As a i/p stage of multistage amplifier	For audio signal amplification	For impedance matching

Typical Transistor Junction Voltages

	$V_{CE(sat)}$	$V_{BE(sat)} = V_\delta$	$V_{BE(active)}$	$V_{BE(cut-in)} = V_\gamma$	$V_{BE(cutoff)}$
Si	0.3	0.7	0.6	0.5	0.0
Ge	0.1	0.3	0.2	0.1	−0.1

} n-p-n transistors at 25°C

Transistor Biasing & Thermal Stabilization

→ **Operating Point:-**

→ In transistor characteristics, the transistor functions most linearly when it operates in active region.

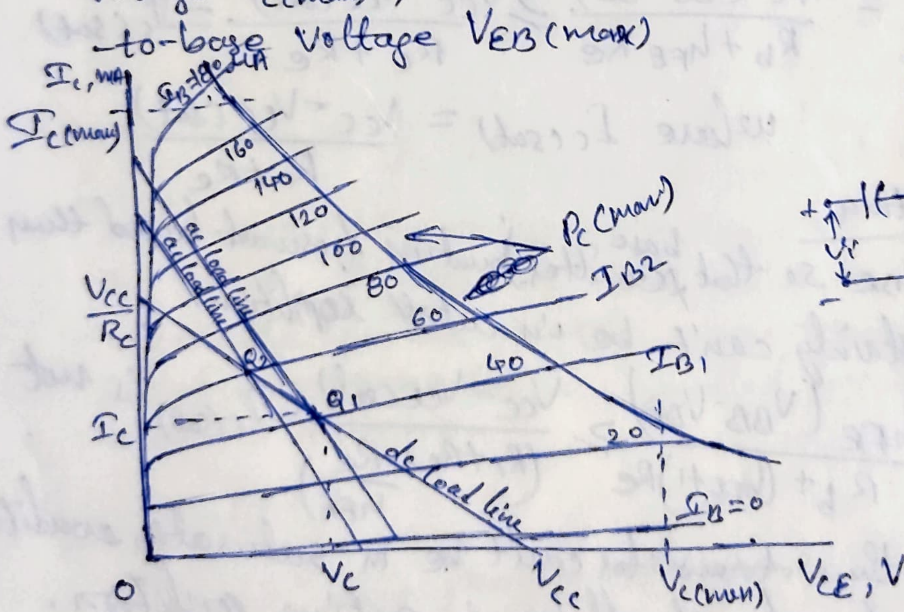
→ To establish an operating point in this region it is necessary to provide appropriate direct potentials & currents, using external sources.

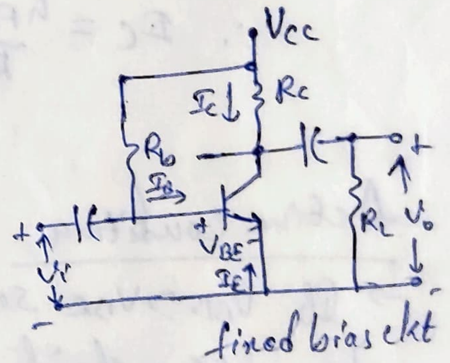
→ Once an operating point Q is established, time-varying excursions of i/p signal (base current) should cause an o/p signal (collector voltage or collector current) of same waveform.

→ If the o/p is not a faithful reproduction of i/p signal, the operating point is unsatisfactory & should be relocated on collector characteristics.

→ Even if we are free to choose R_c, R_L, R_b & V_{cc}, we may not operate the transistor everywhere in the active region because various transistor ratings limit the range of useful operation.

→ These ratings are max. collector dissipation $P_c(max)$, max. collector voltage $V_{c(max)}$, max. collector current $I_{c(max)}$ & max. emitter-to-base voltage $V_{EB(max)}$





→ **dc & ac Load Lines**

→ Since capacitors are open ckted under dc condition, the dc or static load line of ckt represents relation b/w I_c & V_{CE} with a slope of $-\frac{1}{R_c}$

→ If $R_L = \infty$ & if i/p signal (base current) is large & symmetrical, we must locate operating point Q_1 at the centre of load line.
→ In this way collector voltage & current may vary approximately symmetrically around the quiescent values V_C & I_C respectively.
→ If $R_L \neq \infty$, an ac or dynamic load line must be considered.
→ Since the capacitors act as short ckts at the i/p signal freq. the effective load R_L' at collector becomes R_C in parallel with R_L
→ Now, ac or dynamic load line is defined as line which passes through the dc operating point Q_1 & has a slope equal to $-\frac{1}{R_L'}$ corresponding to collector load $R_L' = R_C || R_L$ under ac conditions.

↳ The fixed-bias ckt:

→ The point Q_2 can be established by noting the required current I_{B2} in choosing the resistance R_b so that base current is equal to I_{B2} $\therefore I_B = \frac{V_{CC} - V_{BE}}{R_b} = I_{B2}$

→ The voltage V_{BE} is approxly 0.2V for Ge & 0.6V for a Si transistor in active region.

→ Since V_{CC} is usually much larger than V_{BE}
$$I_B = \frac{V_{CC}}{R_b}$$

→ The current I_B is const. & network is called fixed-bias ckt.

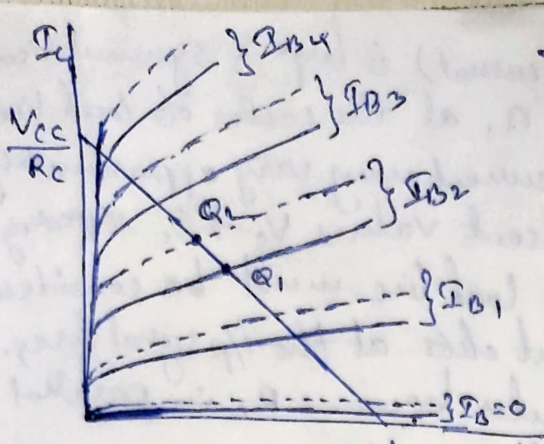
→ The selection of an operating point Q depends upon a no. of factors. They are ac & dc loads on the stage, available power supply, max. transistor rating, peak signal excursions to be handled by stage, & the tolerable distortion.

→ Bias Stability

→ There are some problems of maintaining the operating point stable.

→ Let us consider the fixed bias ckt. in which the base current I_B is kept const. since $I_B \simeq \frac{V_{CC}}{R_b}$

→ Let us assume that the transistor is replaced by another of same type with β greater for replacement transistor.



→ The o/p characteristics increase or decrease (for equal changes in I_B) as β increases or decreases.

→ Since I_B is maintained const. at I_{B2} by external biasing ckt. it follows that the operating point move to Q_2

→ The new operating point may be completely unsatisfactory.

→ We now conclude that maintaining I_B const. will not provide operating-point stability as β changes.

→ So I_B should be allowed to change so as to maintain I_C & V_{CE} const. as β changes.

→ Thermal Instability

→ Second important cause for bias instability is a variation in temperature.

→ I_{CO} doubles for every 10°C rise in temp. which may cause considerable practical difficulty in using a transistor as a ckt element.

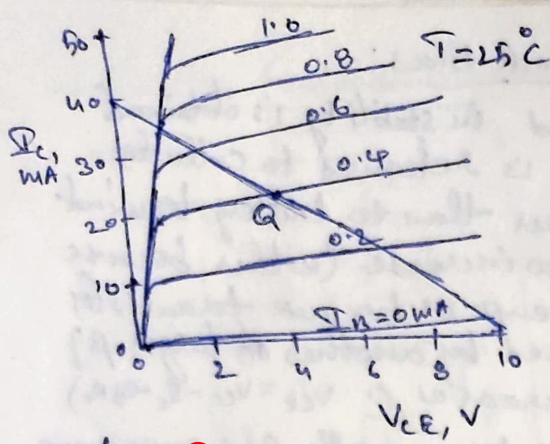
→ The collector current I_C causes the collector-junction temp. to rise, which in turn increases I_{CO}. As a result of growth of I_{CO}, I_C will increase, which may further increase junction temp. & consequently I_{CO}

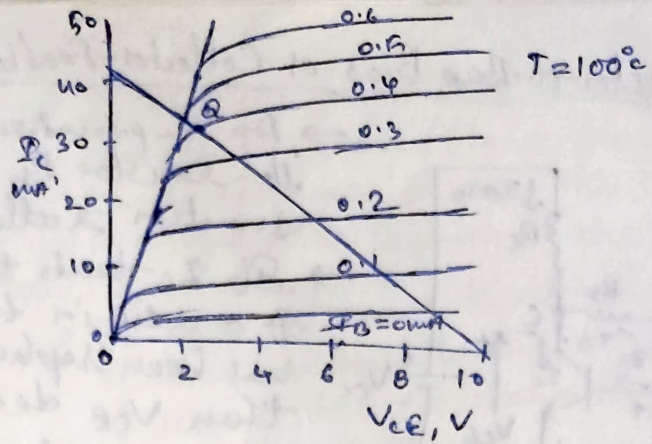
→ This succession of events becomes cumulative, so that the ratings of transistor are exceeded & the device burns out.

→ Even if above changes does not take place, it is possible for a transistor which is biased in active region to find itself in saturation region as a result of this operating point instability

→ If $I_B = 0$ then $I_C = \frac{I_{CO}}{1-\alpha}$. As temp. increases I_{CO} increases, the $I_B=0$ line in CE characteristics will move upward.

→ The characteristics for other values of I_B will also move upward by the same amount (provided β remains const.) & consequently the operating point will move if I_B is forced to remain const.





↳ The Stability Factor S

→ In biasing a transistor in active region we should maintain the operating point stable by keeping I_C & V_{CE} const.

→ The techniques used to do so may be classified in 2 categories: 1) stabilization techniques & 2) Compensation techniques.

→ Stabilization techniques refer to use of resistive biasing ckts which allow I_B to vary so as to keep I_C relatively const. with variations in I_{CO}, β & V_{BE}.

→ Compensation techniques refer to use of temperature-sensitive devices such as diodes, transistors, thermistors, which provide compensating voltages & currents to maintain operating point const.

→ Stability factor S is defined as the rate of change of collector current w.r.t. reverse saturation current, keeping β & V_{BE} const.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}}$$

→ S cannot be smaller than unity.

→ The larger the value of S, the ckt is more likely to exhibit thermal instability.

→ Other stability factors may also be defined as $\frac{\partial I_C}{\partial \beta}$ & $\partial I_C / \partial V_{BE}$

→ In active region $I_C = (1+\beta) I_{CO} + \beta I_B$

→ Differentiate I_C w.r.t I_C considering β const. with I_C then

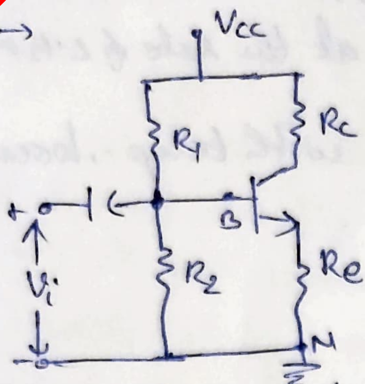
$$1 = \frac{1+\beta}{S} + \beta \frac{dI_B}{dI_C}$$

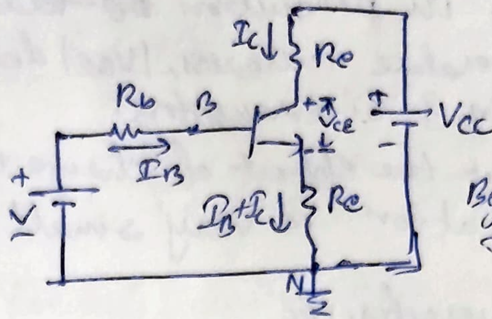
$$\Rightarrow S = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_C}\right)}$$

→ For fixed bias ckt I_B is independent of I_C. Hence the stability factor $S = 1+\beta$

→ Self-Bias, Emitter Bias or Voltage-Divide Bias

→





By use of Thevenin's theorem

→ A ckt which can be used even if there is zero dc resistance in series with collector terminal is self-biasing configuration.

→ The current in resistance Re in emitter lead causes a voltage drop which is in the direction to reverse-bias the emitter junction.

→ Since emitter junction must be forward-biased, the base voltage is obtained from supply through $R_1 R_2$ network.

→ If $R_b = R_1 || R_2 \to 0$, then base to ground voltage V_{BN} is independent of I_{C0}. For best stability R_1 & R_2 must be kept as small as possible.

→ If I_C tends to increase, the current in Re increases

→ As a consequence of increase in voltage drop across Re, the base current is decreased. Hence I_C will increase less than it would had been with no self-biasing resistor Re

→ Stability Factor, S

$$V = \frac{R_2 V_{CC}}{R_1 + R_2} \qquad R_b = \frac{R_2 R_1}{R_1 + R_2}$$

$$V = I_B R_b + (I_B + I_C) R_e + V_{BE}$$

$$\Rightarrow I_B = \frac{V - V_{BE} - I_C R_e}{R_b + R_e} \Rightarrow \frac{dI_B}{dI_C} = -\frac{R_e}{R_e + R_b}$$

$$S = \frac{1+\beta}{1 - \beta \frac{dI_B}{dI_C}} = \frac{1+\beta}{1 + \beta \frac{R_e}{R_e + R_b}} = \frac{(1+\beta)(R_e + R_b)}{R_e + R_b + \beta R_e}$$

$$= (1+\beta) \frac{1 + R_b/R_e}{1 + \beta + R_b/R_e}$$

→ S varies b/w 1 for small R_b/R_e & $(1+\beta)$ for $R_b/R_e \to \infty$

⇒ The smaller the value of R_b, the better the stabilization.

→ Stabilization Against Variations in V_{BE} and β for Self-Bias Circuit

→ Two other sources of instability in I_C are due to variation of V_{BE} & β with temperature & with manufacturing tolerances in production of transistors.

→ As temperature increases, $|V_{BE}|$ decreases at the rate of 2.5 mV/°C for both Ge & Si transistors.

→ We neglect the effect of change of V_{CE} with temp., because this variation is very small

↳ Transfer Characteristic

→ $$V = I_B R_b + V_{BE} + (I_B + I_C) R_e$$

$$\Rightarrow V_{BE} = V - I_B(R_b + R_e) - I_C R_e$$

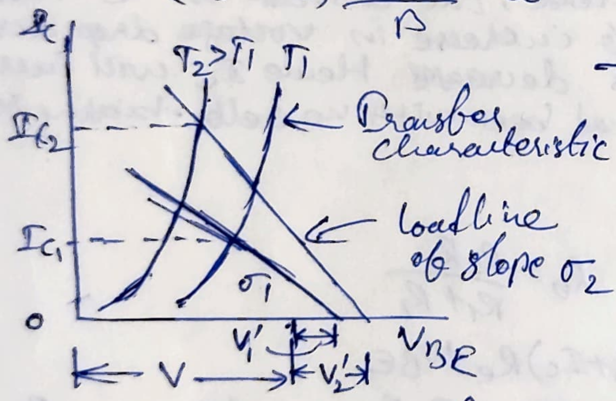
→ We have $I_C = (1+\beta) I_{C0} + \beta I_B \Rightarrow I_B = \frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{C0}$

$$\Rightarrow V_{BE} = V - \left(\frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{C0}\right)(R_b + R_e) - I_C R_e$$

$$\therefore V_{BE} = V + (R_b + R_e) \frac{\beta+1}{\beta} I_{C0} - \frac{R_b + R_e(1+\beta)}{\beta} I_C$$

→ This equation represents a load line in $I_C - V_{BE}$ plane with intercept on V_{BE} axis is $V + V'$, where

$$V' = (R_b + R_e) \frac{\beta+1}{\beta} I_{C0} = (R_b + R_e) I_{C0} \quad (\because \beta >> 1)$$



→ If at $T = T_1 (T_2)$ $I_C = I_{C01} (I_{C02})$ & $\beta = \beta_1 (\beta_2)$ then $V_1' = (R_b + R_e) I_{C01}$ & $V_2' = (R_b + R_e) I_{C02}$

→ Hence the intercept of load line on V_{BE} axis is a function of temp. because I_{C0} increases with T

→ The slope of load line is $\sigma = \frac{-\beta}{R_b + R_e(1+\beta)}$ & hence $|\sigma|$ increases with T because β increases with T.

→ The intersection of load line with transfer characteristic gives the collector current I_C

↳ Stability factor S'

→ The variation of I_C with V_{BE} is given by the stability factor S', denoted by $S' \equiv \frac{\partial I_C}{\partial V_{BE}}$ where both I_{C0} & β are considered consts

→ For self bias ckt $V_{BE} = V + (R_b + R_e)\frac{\beta+1}{\beta} I_{CO} - \frac{R_b + R_e(1+\beta)}{\beta} I_C$

→ Differentiating with V_{BE} on both sides with I_{CO} & β const

$$1 = -\frac{R_b + R_e(1+\beta)}{\beta} S'$$

$$\Rightarrow S' = \frac{-\beta}{R_b + R_e(1+\beta)} = \frac{-\beta}{1+\beta} \cdot \frac{S}{R_b + R_e}$$

→ As we reduce S towards unity, we can minimize ~~the~~ change of I_C w.r.t. both V_{BE} & I_{CO}

↳ The stability Factor S''

→ The variation of I_C w.r.t. β is given by stability factor S'' defined by $S'' = \frac{\partial I_C}{\partial \beta}$ where both I_{CO} & V_{BE} are considered const.

→ For self bias ckt $V_{BE} = V + V' - \frac{R_b + R_e(1+\beta)}{\beta} I_C$

$$\Rightarrow I_C = \frac{\beta(V + V' - V_{BE})}{R_b + R_e(1+\beta)}$$

where V' may be taken to be independent of β.

→ On differentiation with β

$$S'' = ~~\frac{V+V'-V_{BE}}{R_b+R_e(1+\beta)}~~ =$$

$$= (V+V'-V_{BE})\left[\frac{(R_b + R_e(1+\beta)) - \beta R_e}{(R_b + R_e(1+\beta))^2}\right]$$

$$= \frac{(V+V'-V_{BE})}{R_b + R_e(1+\beta)} \cdot \frac{R_e + R_b}{R_b + R_e(1+\beta)}$$

$$= \frac{I_C}{\beta} \cdot \frac{S}{(1+\beta)}$$

→ The change in collector current due to change in β is

$$\Delta I_C = S'' \Delta\beta = \frac{I_C S}{\beta(1+\beta)} \Delta\beta$$

where $\Delta\beta = \beta_2 - \beta_1$ may represent a large change in β

→ $$S'' = \frac{I_{C2} - I_{C1}}{\beta_2 - \beta_1} = \frac{\Delta I_C}{\Delta\beta}$$

→ We have $\frac{I_{C2}}{I_{C1}} = \frac{\beta_2}{\beta_1} \frac{R_b + R_e(1+\beta_1)}{R_b + R_e(1+\beta_2)}$ $\left(\because I_C = \frac{\beta(V+V'-V_{BE})}{R_b + R_e(1+\beta)}\right)$