GNITS-R- 18 –113AT

G. Narayanamma Institute of Technology & Science

(**Autonomous**) ***(for Women)***

Shaikpet, Hyderabad- 500 104

II-B.Tech I-Semester *Regular Examinations, Dec*-2019.

DIGITAL SYSTEM DESIGN

*(Common to ECE & ETE***)**

Max. Marks: 70 **Time: 03 Hours**

Note:

1. Question paper comprises of **Part A** and **Part B**.
2. **Part A** is compulsory which carries 10 marks. Answer all questions in Part A.
3. **Part B** (for 60 marks) consists of **five questions** with **"either" "or"** pattern. Each question carries 12 marks and may have a,b,c as sub questions. The student has to answer any one full question.

PART-A

*(Answer 05 questions. Each question carries **2 marks**)*

[5x2= 10]

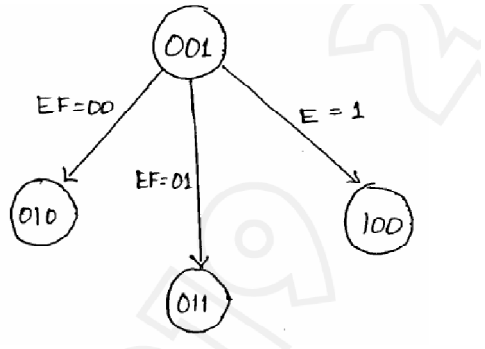
Q.No	Question	Marks	Bloom's Level
Q.1	a) Why is a hexadecimal system called an alpha numeric number system?	**[2]**	**L1**
	b) Why commercial ECL families are not as popular as CMOS and TTL?	**[2]**	**L2**
	c) What are the advantages of tabulation method over K-map?	**[2]**	**L1**
	d) Explain Clock Skew and define Level triggering, Edge triggering modes of operation.	**[2]**	**L1**
	e) Differentiate between Mealy and Moore machines.	**[2]**	**L1**

END OF PART A

PART-B

*(Answer **05** full questions. Each question carries **12 marks**)*

Q.No	Question	Marks	Bloom's Level
Q.2(a)	Represent and draw the following Boolean functions using minimum number of basic gates. i) (AB + AB') (AB)' ii) [(ABD(C + D + E)) + (A +DBC)'] (ABC + (CAD)')	**[07]**	**L3**
(b)	Convert the following numbers i) $(1FA.B)_{16}$ to base 8 ii) $(549.7)_{10}$ to binary. iii) $(111001101.110010)_2$ to octal.	**[05]**	**L2**
	OR		
Q.3(a)	Define the following types of codes and give an example for it i) Weighted code ii) Non-weighted code iii) Self complementing code iv) Cyclic code	**[07]**	**L1**
(b)	Perform the following addition using excess-3 code i) $(386)_{10}+(756)_{10}$ ii) $(1010)_{10} + (444)_{10}$.	**[05]**	**L3**

Q.4(a)	Explain about CMOS/ECL interfacing	**[06]**	**L2**
(b)	Design a 2-input NAND logic gate using TTL and explain its operation.	**[06]**	**L1**
	OR		
Q.5(a)	Design a transistor circuit for 2 input ECL NOR gate and explain circuit with the help of logic diagrams and function table.	**[06]**	**L1**
(b)	Design a 2-input XOR and XNOR logic gates using CMOS logic	**[06]**	**L3**
Q.6(a)	Simplify the given Boolean function F(w, x, y, z) = Σ(2, 3, 12, 13, 14, 15) using i) Sum of Products and ii) Product of Sums K-Map representation and implement using only NAND Gates.	**[08]**	**L2**
(b)	What is the difference between canonical form and standard form? Which form is preferable while implementing a Boolean function with gates?	**[04]**	**L1**
	OR		
Q.7(a)	Given F(A,B,C,D) = Σ(1, 4, 6, 7, 8, 9, 10, 11, 15). Simplify using Quin-McClusky method and determine the prime implicants, essential prime implicants and the minimized Boolean expression.	**[08]**	**L2**
(b)	Compare PROM, PLA and PAL.	**[04]**	**L1**
Q.8(a)	Explain the conversion procedure from one flip flop to another flip flop with the help of JK to D conversion.	**[07]**	**L2**
(b)	What is race around condition how can it be eliminated?	**[05]**	**L1**
	OR		
Q.9(a)	Design a divide by 16 synchronous down counter.	**[07]**	**L2**
(b)	What is the propagation delay in asynchronous counters? Explain how it effects maximum clock frequency?	**[05]**	**L4**
Q.10(a)	Draw the ASM chart for the following state diagram 	**[07]**	**L3**
(b)	Explain the capabilities and limitations of fine state machines.	**[05]**	**L1**
	OR		
Q.11	Design a binary multiplier and its control logic by drawing ASM chart and realize the same using gates and D Flip-Flops.	**[12]**	**L2**

END OF PART B

END OF THE QUESTION PAPER