GNITS-R- 18 – 113AT

G. Narayanamma Institute of Technology & Science

(**Autonomous**) ***(for Women)***

Shaikpet, Hyderabad- 500 104

II-B.Tech I-Semester *Regular/Supplementary Examinations, Feb/Mar*-2023.

DIGITAL SYSTEM DESIGN

***(Common to ECE & ETE*)**

Max. Marks: 70 **Time: 03 Hours**

Note:

1. Question paper comprises of **Part A** and **Part B**.
2. **Part A** is compulsory which carries 10 marks. Answer all questions in Part A.
3. **Part B** (for 60 marks) consists of **five questions** with **"either" "or"** pattern. Each question carries 12 marks and may have a,b,c as sub questions. The student has to answer any one full question.

PART-A

*(Answer 05 questions. Each question carries **2 marks**)*

Q.No	Question	Marks	CO	Bloom's Level
Q.1	a) Perform the following using 2's compliment method i)$14.68_{(10)} + 228.134_{(10)}$ ii) $112.65_{(10)} - 347.31_{(10)}$	**[02]**	**CO**	**[L2]**
	b) List the advantages of CMOS logic family	**[02]**	**CO**	**[L1]**
	c) Draw the circuit which generate even parity for 3-bit input.	**[02]**	**CO**	**[L1]**
	d) What is race around condition? When and why does it occur?	**[02]**	**CO**	**[L1]**
	e) Draw the general structure of Meely and Moore machines.	**[02]**	**CO**	**[L1]**

END OF PART-A

PART-B

*(Answer **05** full questions. Each question carries **12 marks**)*

Q.No	Question	Marks	CO	Bloom's Level
Q.2(a)	Realize the given function i) using only NOR gates ii) Using Fundamental gates. F = (x' + y' + z).(x' + y + z) .(x + y' + z'). (x + y'+ z)	**[08]**	**CO**	**[L2]**
(b)	Simplify the expression f= w'x(z'+y'z) + x(w+w'yz) using Boolean algebra postulates to one literal and draw the truth table.	**[04]**	**CO**	**[L3]**
	OR			
Q.3(a)	Find the complement of the function and express them in Canonical POS and SOP form F= AB + A(B+C) + B'(B+D)	**[08]**	**CO**	**[L2]**
(b)	State and prove Consensus theorem. Simplify the following function using consensus theorem w'y' + wyz + xy'z +wx'y.	**[04]**	**CO**	**[L3]**

Q.4(a)	Explain about sinking and sourcing currents in TTL family.	**[04]**	**CO**	**[L1]**

(b)	Draw and Explain the operation of 2 input AND gate using CMOS logic.	**[08]**	**CO**	**[L2]**
	OR			
Q.5(a)	With neat diagram explain the operation of 2 input NOR gate using TTL logic.	**[06]**	**CO**	**[L2]**
(b)	Explain how to interface CMOS/TTL logic families.	**[06]**	**CO**	**[L2]**

Q.6(a)	Construct the 16 x 1 Mux using 8 x 1 Mux.	**[04]**	**CO**	**[L3]**
(b)	Design a combinational circuit which takes 3 bit binary input and gives its output as square of its input.	**[08]**	**CO**	**[L3]**
	OR			
Q.7(a)	Construct a combinational logic circuit which converts a decimal number into an equivalent Excess-3 number.	**[08]**	**CO**	**[L3]**
(b)	Implement Full adder using PLA and PAL.	**[04]**	**CO**	**[L2]**

Q.8(a)	Construct synchronous BCD Counter and explain its operation.	**[08]**	**CO**	**[L3]**
(b)	Compare BCD counter and Decade counter.	**[04]**	**CO**	**[L2]**
	OR			
Q.9(a)	Design a synchronous counter with T flip-flop that goes through the sequence 0,1,3,7,6,4,0,1….	**[08]**	**CO**	**[L3]**
(b)	Draw the circuit of Universal shift register.	**[04]**	**CO**	**[L1]**

Q.10(a)	Develop the state diagram of serial binary adder and explain the methodology	**[08]**	**CO**	**[L6]**
(b)	Analyze and explain the steps involved in the synthesis of synchronous sequential circuit.	**[04]**	**CO**	**[L1]**
	OR			
Q.11(a)	Develop an ASM chart to implement the function of a Dice game Controller.	**[08]**	**CO**	**[L6]**
(b)	Define setup time and hold time. Explain their importance in the design of sequential circuits	**[04]**	**CO**	**[L2]**

END OF PART B

END OF THE QUESTION PAPER