GNITS-R-18- 113AT

G. Narayanamma Institute of Technology & Science

(**Autonomous**) ***(for Women)***

Shaikpet, Hyderabad- 500 104

II-B.Tech I-Semester *Regular Examinations, March-2021*.

DIGITAL SYSTEM DESIGN

***(Common to ECE & ETE*)**

Max. Marks: 70 **Time: 03 Hours**

(Answer any 05 full questions. Each question carries 14 marks)

****

Q.No	Question	Marks	Bloom's Level
Q.1(a)	Solve A – B using 2's complement if i) A = $(111.101)_2$ and B = $(101.110)_2$ ii) A = $(27)_8$ and B = $(16)_8$	**[07]**	**[L3]**
(b)	State and prove the Consensus theorem and De-Morgan's theorem with suitable examples.	**[07]**	**[L2]**
Q.2	Realize the following expression F(A,B,C,D) =∑m(0,1,2,3,4,7,9,11) using the following two level forms i) NAND-NAND ii) AND-OR iii) OR-AND iv) NOR-NOR	**[14]**	**[L3]**
Q.3(a)	Draw and explain TTL NAND logic with the help of truth table.	**[07]**	**[L3]**
(b)	Explain how a CMOS can be interfaced with ECL.	**[07]**	**[L2]**
Q.4(a)	Design a CMOS NAND and XNOR gates and explain the operation of the circuits.	**[08]**	**[L4]**
(b)	Compare CMOS, TTL and ECL with reference to digital IC constraints.	**[06]**	**[L2]**
Q.5(a)	Minimize the following Boolean expression using tabular method and realize using basic gates. F (A, B, C, D) =∑m (0,2,4,9,12,15)+ ∑ d(1,5,7,10)	**[08]**	**[L3]**
(b)	Explain the operation of a 8x1 multiplexer with appropriate expression.	**[06]**	**[L2]**
Q.6(a)	Design a Binary to Gray code converter and realize the logic diagram.	**[08]**	**[L6]**
(b)	Differentiate PROM, PLA and PAL.	**[06]**	**[L2]**
Q.7(a)	Explain the operation of a Master-Slave JK flip flop with suitable timing Diagrams.	**[08]**	**[L1]**
(b)	Design a Serial Input – Parallel Output Shift Register and explain the operation.	**[06]**	**[L2]**
Q.8(a)	Draw an ASM chart to implement the function of Dice Game Controller.	**[08]**	**[L4]**
(b)	Explain the advantages of ASM over Conventional Flow Chart.	**[06]**	**[L1]**

---00O00---